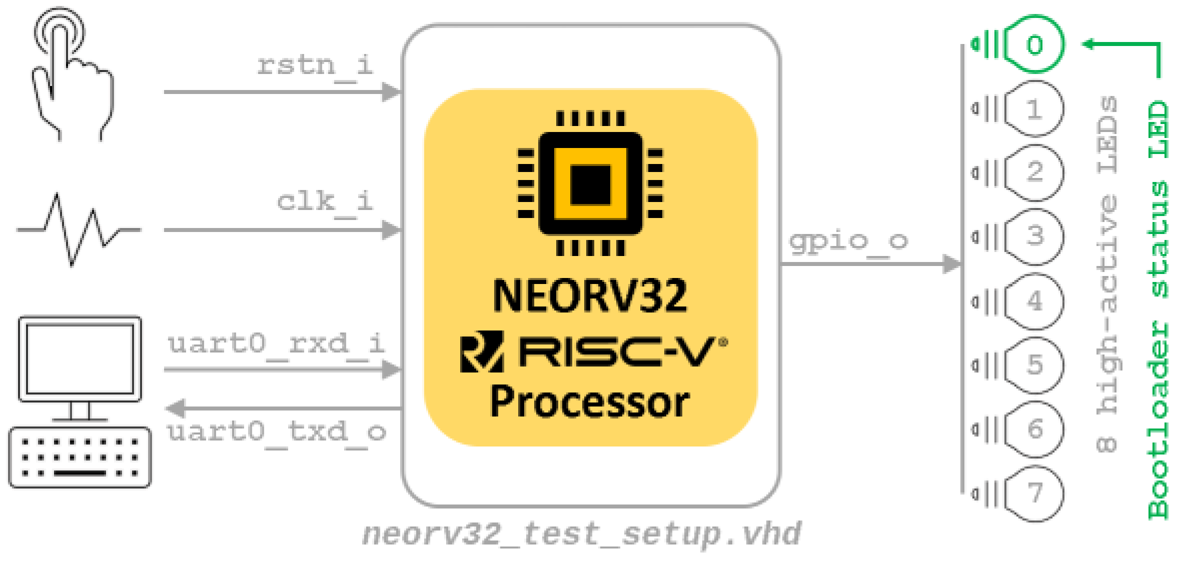
RISC-V tutorial

This tutorial will guide you to implement the RISC-V “neorv32” processor on the Zybo Z7 board and set the RISC-V compiler toolchain on Ubuntu.



You can find additional information for the NEORV-32 microarchitecture in the following links

https://stnolting.github.io/neorv32/

https://stnolting.github.io/neorv32/ug/

https://github.com/stnolting/neorv32/tree/v1.7.2

Hardware implementation

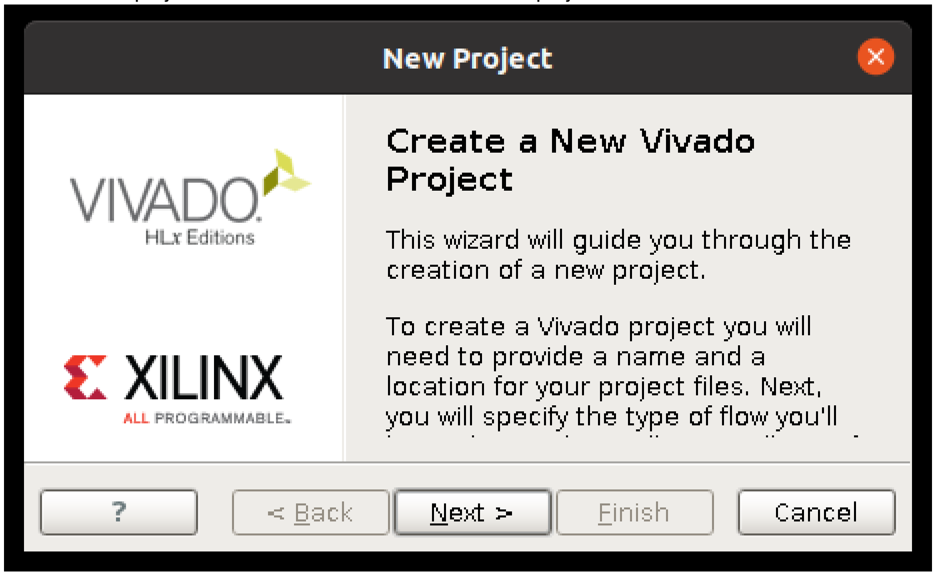
- First, we should download the VHDL source code of the NEORV-32.
- Open a terminal and type the following:

```
cd
mkdir -p wsp
cd wsp
git clone https://github.com/stnolting/neorv32.git
cd neorv32/
git checkout v1.8.0
```

- Beautiful, we now have the source code for NEORV-32. Let’s open Vivado to implement the processor
- Open Vivado

```
cd
cd wsp
mkdir -p vivado_projects
cd vivado_projects
source /opt/Xilinx/Vivado/2016.4/settings64.sh
vivado &
```

- Create a new project. Click from Vivado menu File New project and click on the next button

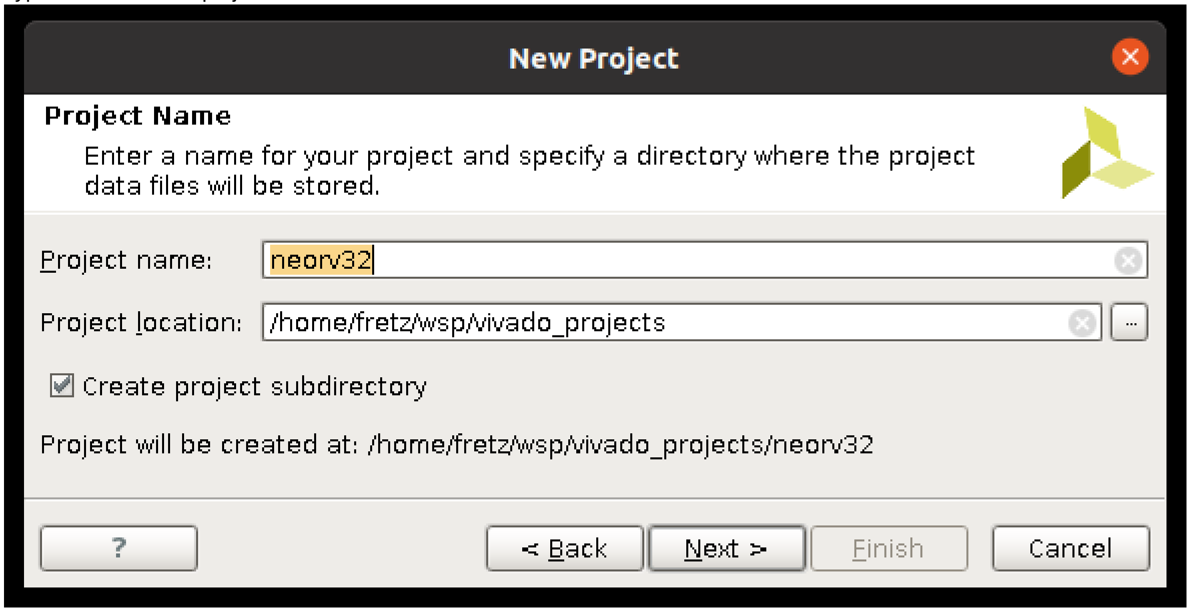


Create a New Vivado Project

This wizard will guide you through the creation of a new project.

To create a Vivado project you will need to provide a name and a location for your project files. Next, you will specify the type of flow you'll

- Type neorv32 as the project name



Project Name

Enter a name for your project and specify a directory where the project data files will be stored.

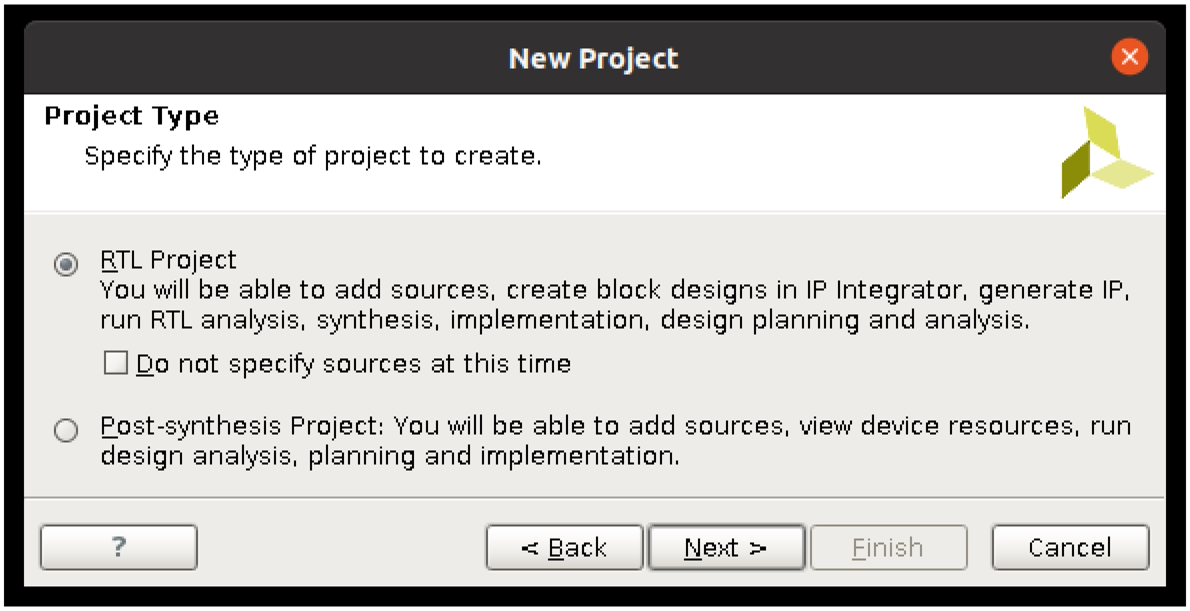
Project name: neorv32

Project location: /home/fretz/wsp/vivado_projects

☑ Create project subdirectory

Project will be created at: /home/fretz/wsp/vivado_projects/neorv32

- Choose the RTL project



New Project

Project Type

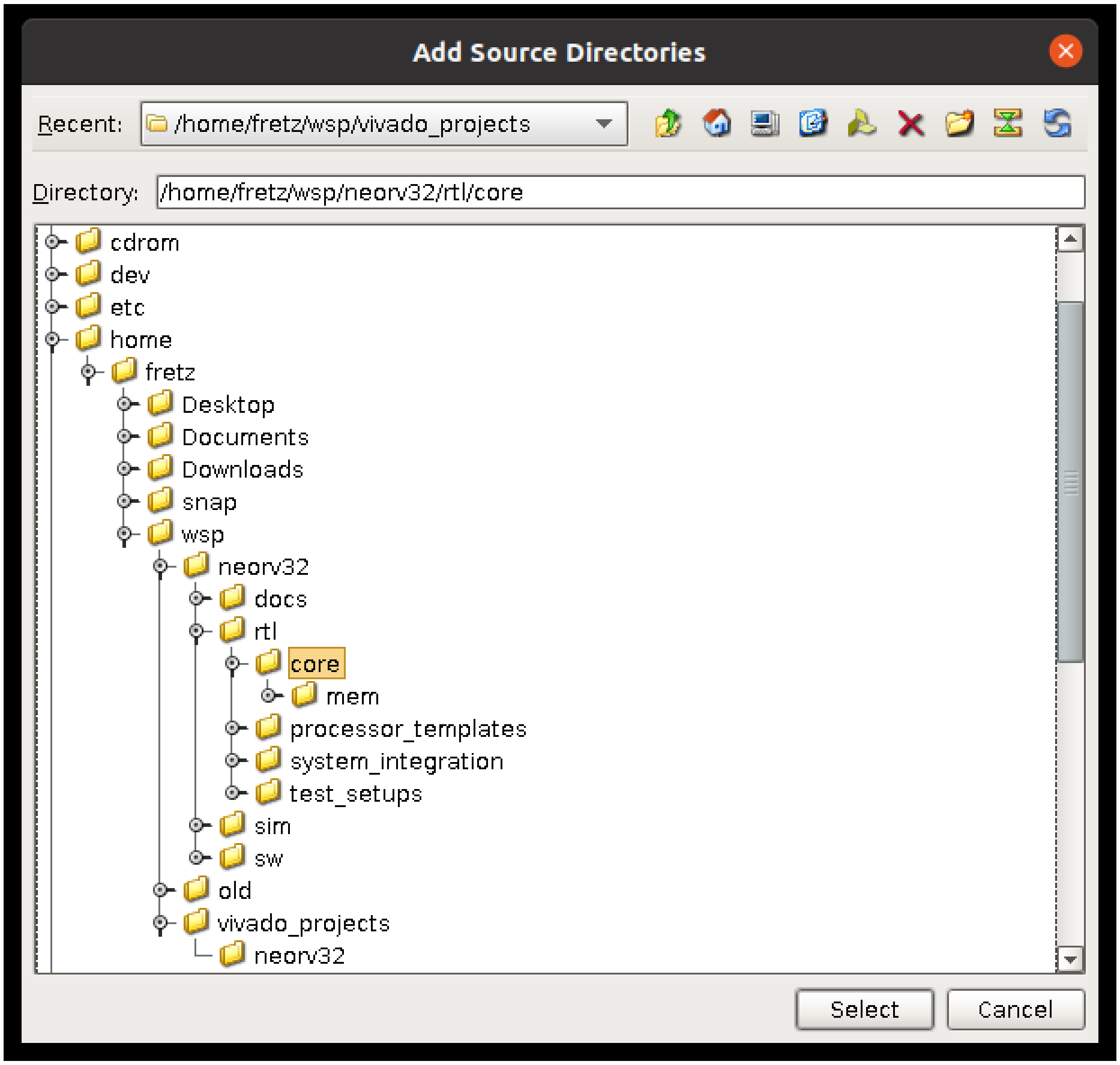
Specify the type of project to create.

[✓ RTL Project]
You will be able to add sources, create block designs in IP Integrator, generate IP, run RTL analysis, synthesis, implementation, design planning and analysis.

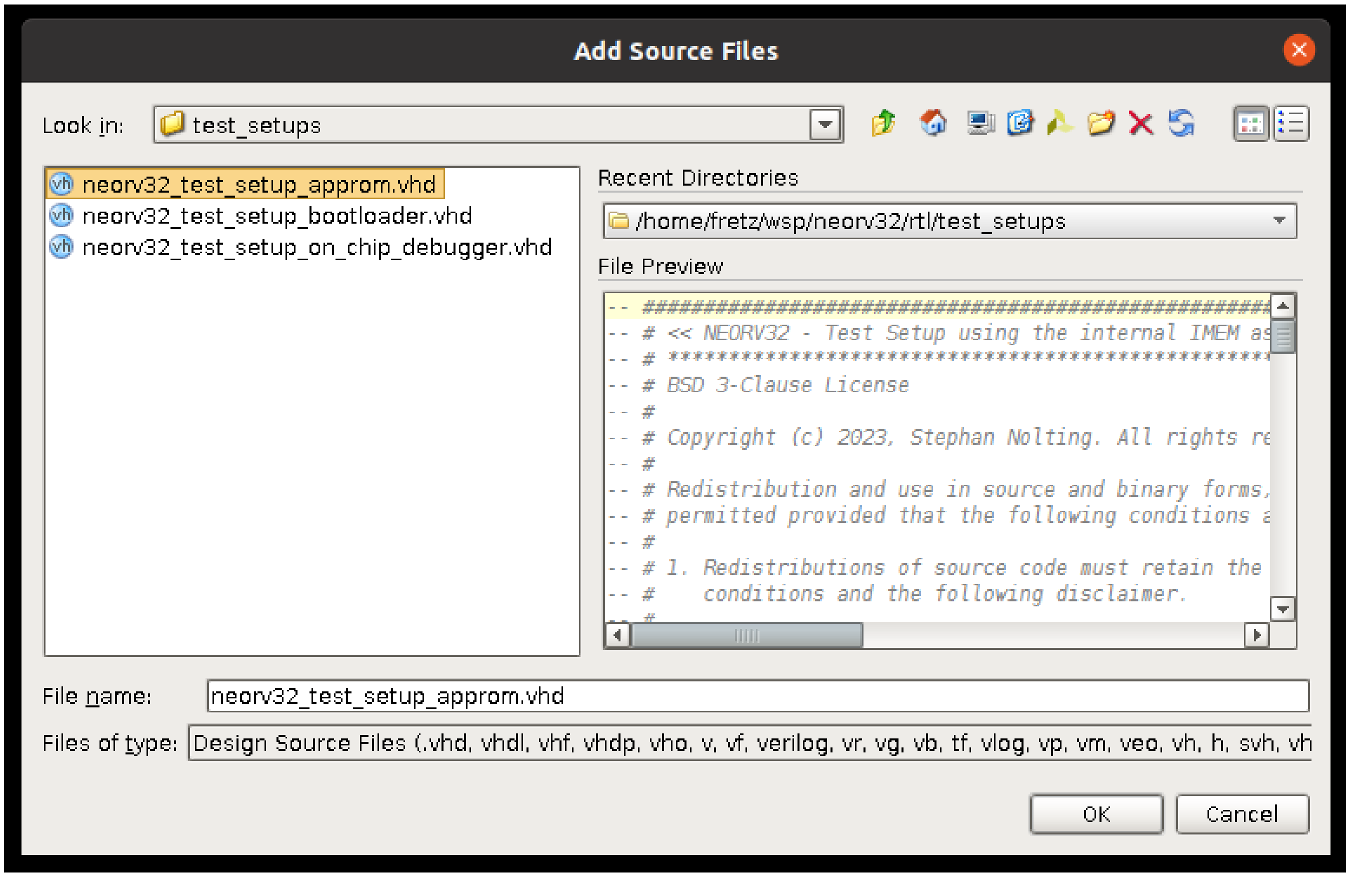
☐ Do not specify sources at this time

Post-synthesis Project: You will be able to add sources, view device resources, run design analysis, planning and implementation.

- Choose as target language **VHDL** and click on the **Add Directories** button to add the VHDL source code of the NEORV-32
- Choose the Directory `/home/fretz/wsp/neorv32/rtl/core/`
-



- Click on the **Add Files** button to add one more source code. Choose `/home/fretz/wsp/neorv32/rtl/test_setups /neorv32_test_setup_bootloader.vhd` and click on the OK button



Look in: test_setups

- neorv32_test_setup_approm.vhd
- neorv32_test_setup_bootloader.vhd
- neorv32_test_setup_on_chip_debugger.vhd

Recent Directories: /home/fretz/wsp/neorv32/rtl/test_setups

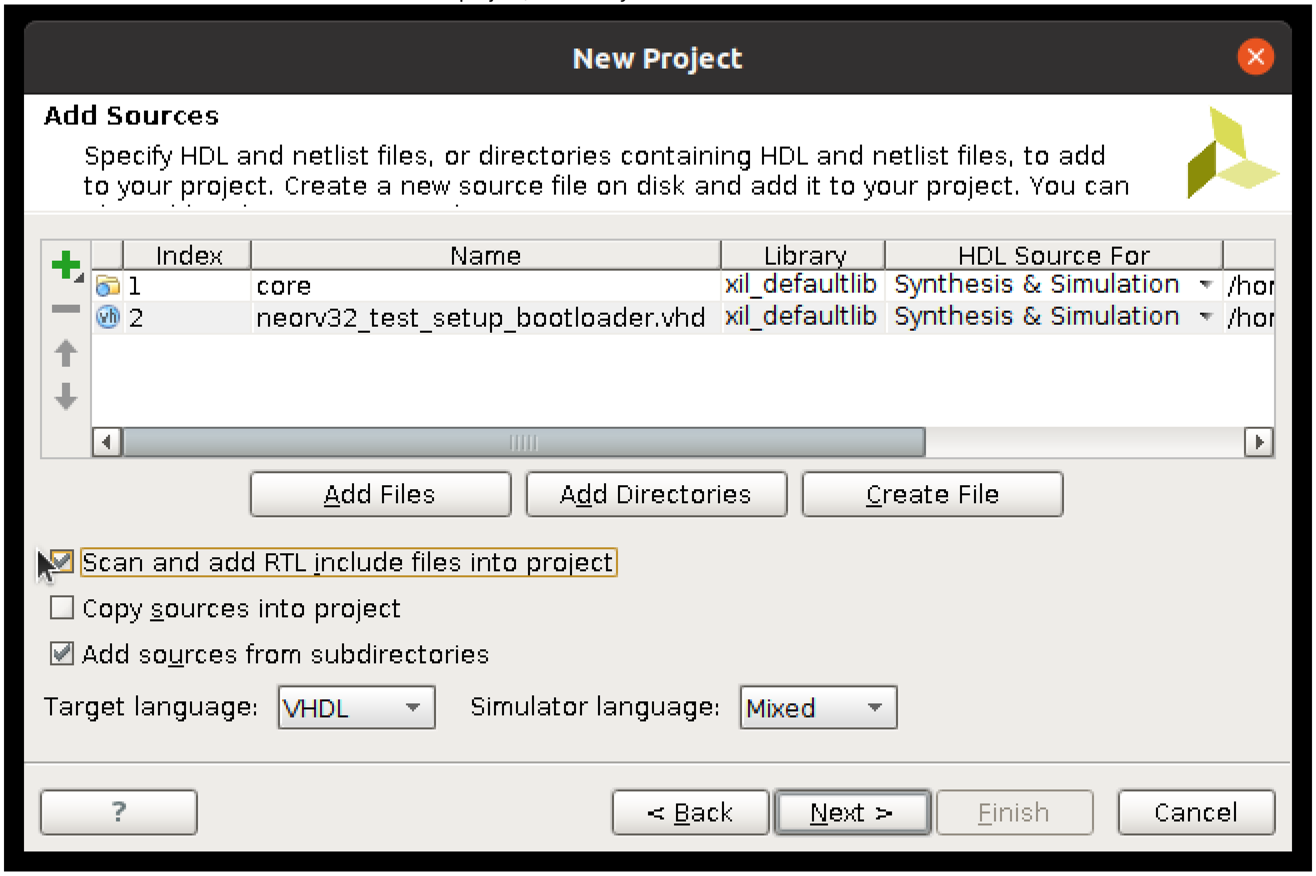
File Preview

```
-- ##################################################################
-- # << NEORV32 - Test Setup using the internal IMEM as
-- # *****************************************************************
-- # BSD 3-Clause License
-- #
-- # Copyright (c) 2023, Stephan Nolting. All rights re
-- #
-- # Redistribution and use in source and binary forms,
-- # permitted provided that the following conditions a
-- #
-- # 1. Redistributions of source code must retain the
-- #    conditions and the following disclaimer.
```

File name: neorv32_test_setup_approm.vhd

Files of type: Design Source Files (.vhd, vhdl, vhf, vhdp, vho, v, vf, verilog, vr, vg, vb, tf, vlog, vp, vm, veo, vh, h, svh, vh

- Tick the Scan and add RTL include files into the project, and finally click on the NEXT button



Add Sources

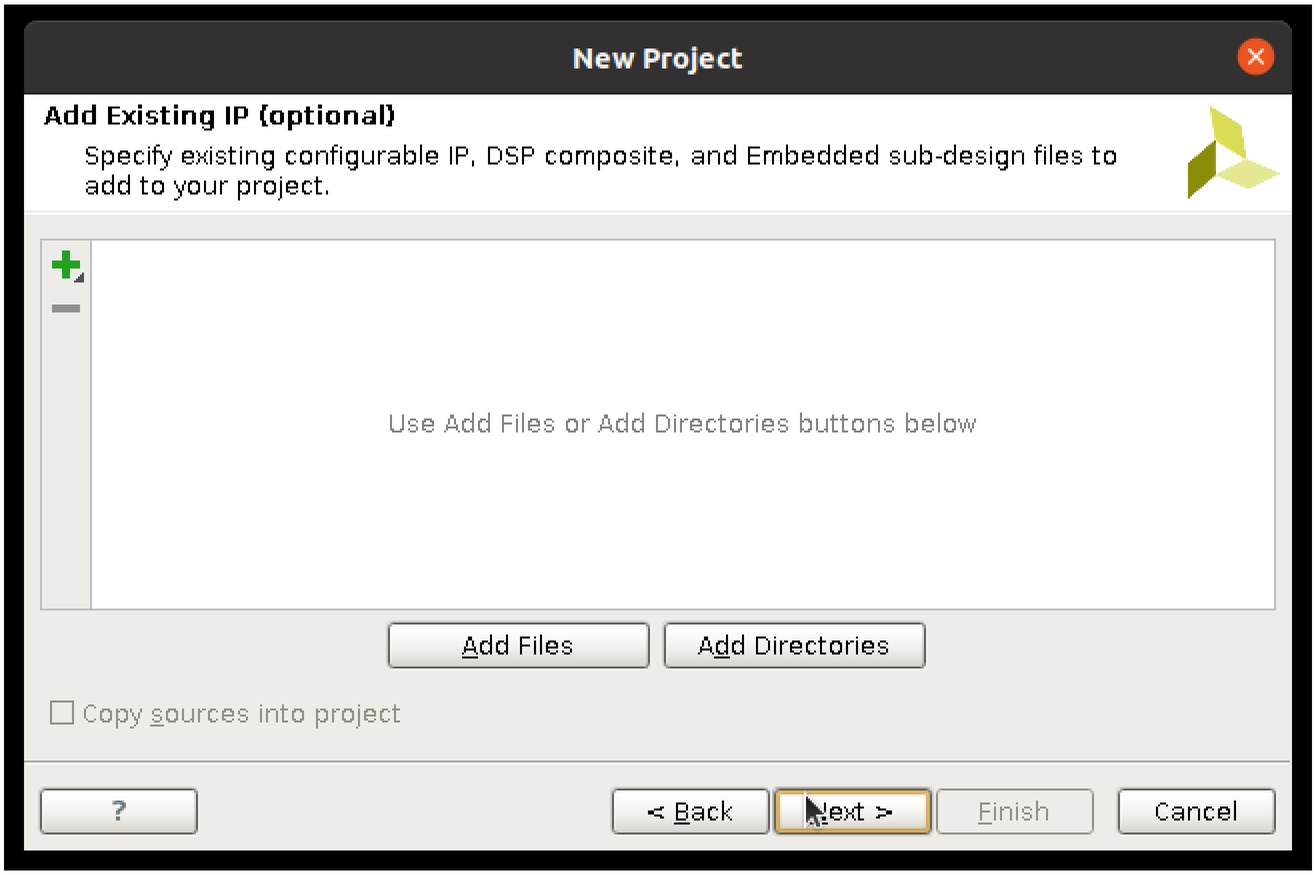
Specify HDL and netlist files, or directories containing HDL and netlist files, to add to your project. Create a new source file on disk and add it to your project. You can

Index	Name	Library	HDL Source For	
1	core	xil_defaultlib	Synthesis & Simulation	/hor
2	neorv32_test_setup_bootloader.vhd	xil_defaultlib	Synthesis & Simulation	/hor

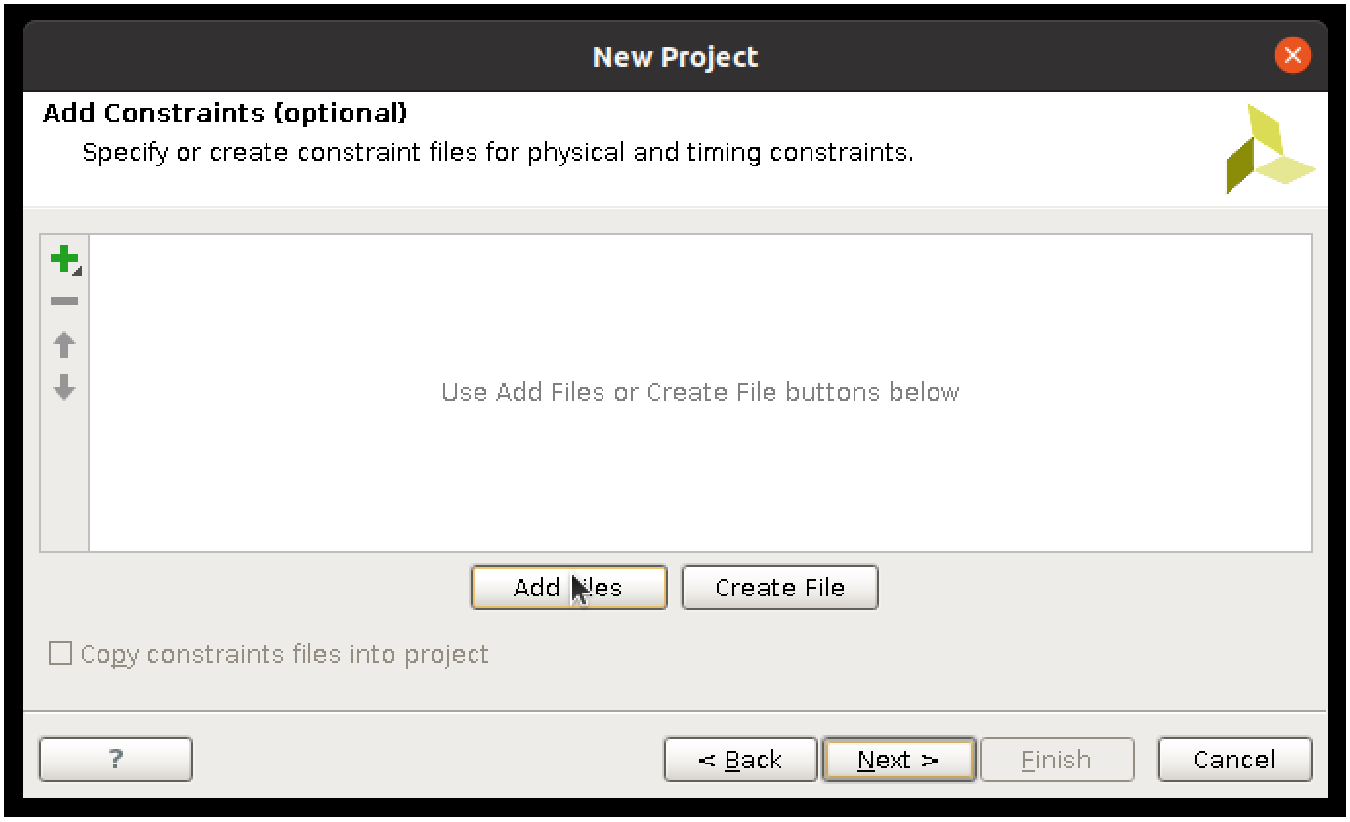
- [✓] Scan and add RTL include files into project
- [ ] Copy sources into project
- [✓] Add sources from subdirectories

Target language: VHDL Simulator language: Mixed

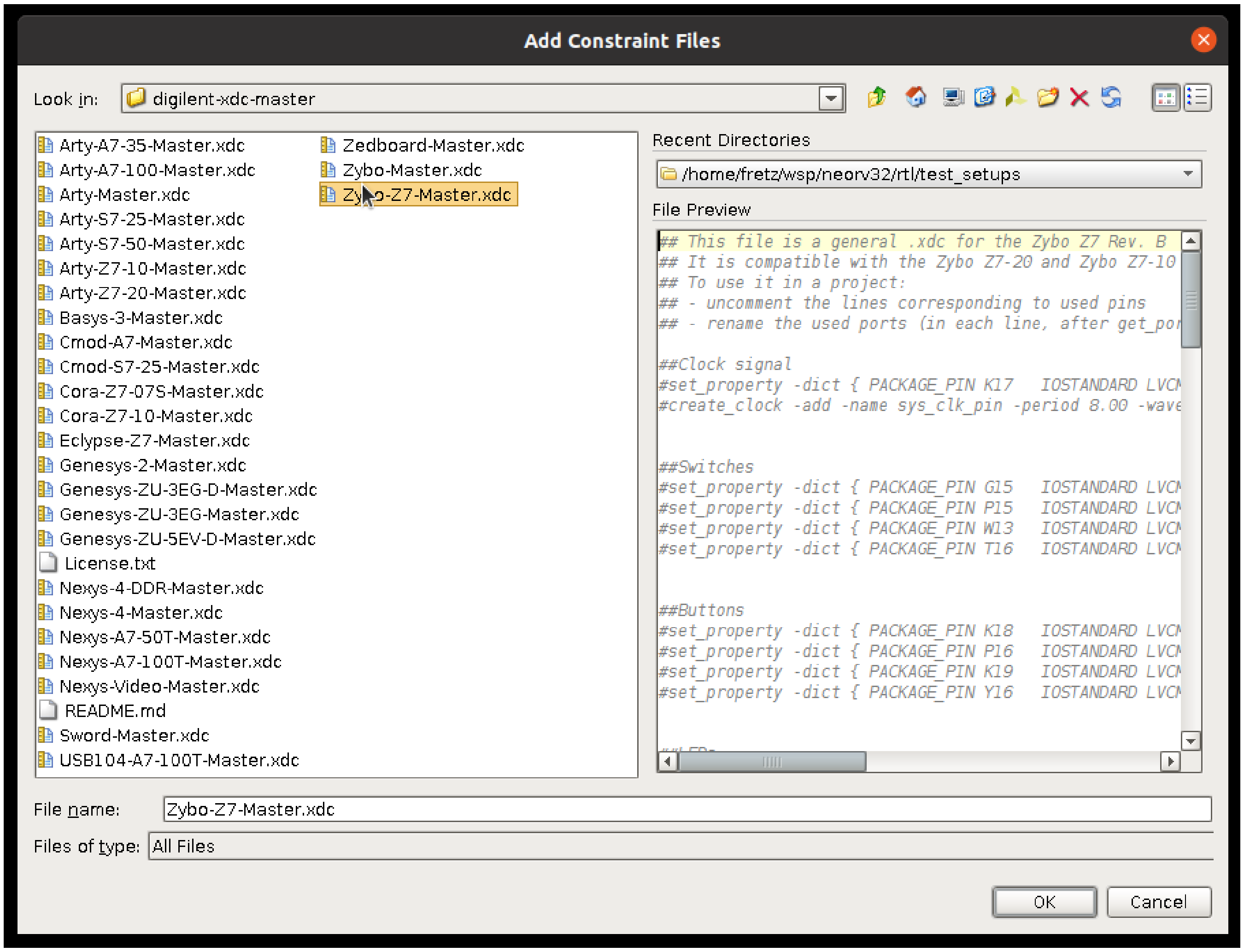
- Click next on the Add Existing IP (optional)


New Project
Add Existing IP (optional)
Specify existing configurable IP, DSP composite, and Embedded sub-design files to add to your project.
Use Add Files or Add Directories buttons below
Add Files
Add Directories
Copy sources into project
?
< Back
Next >
Finish
Cancel

- Click on the Add Files on the Add Constraints window


New Project
Add Constraints (optional)
Specify or create constraint files for physical and timing constraints.
Use Add Files or Create File buttons below
Add Files
Create File
Copy constraints files into project
?
< Back
Next >
Finish
Cancel

- Choose the `/home/fretz/wsp/Downloads/digilent-xdc-master/Zybo-Z7-Master.xdc`and press the OK button



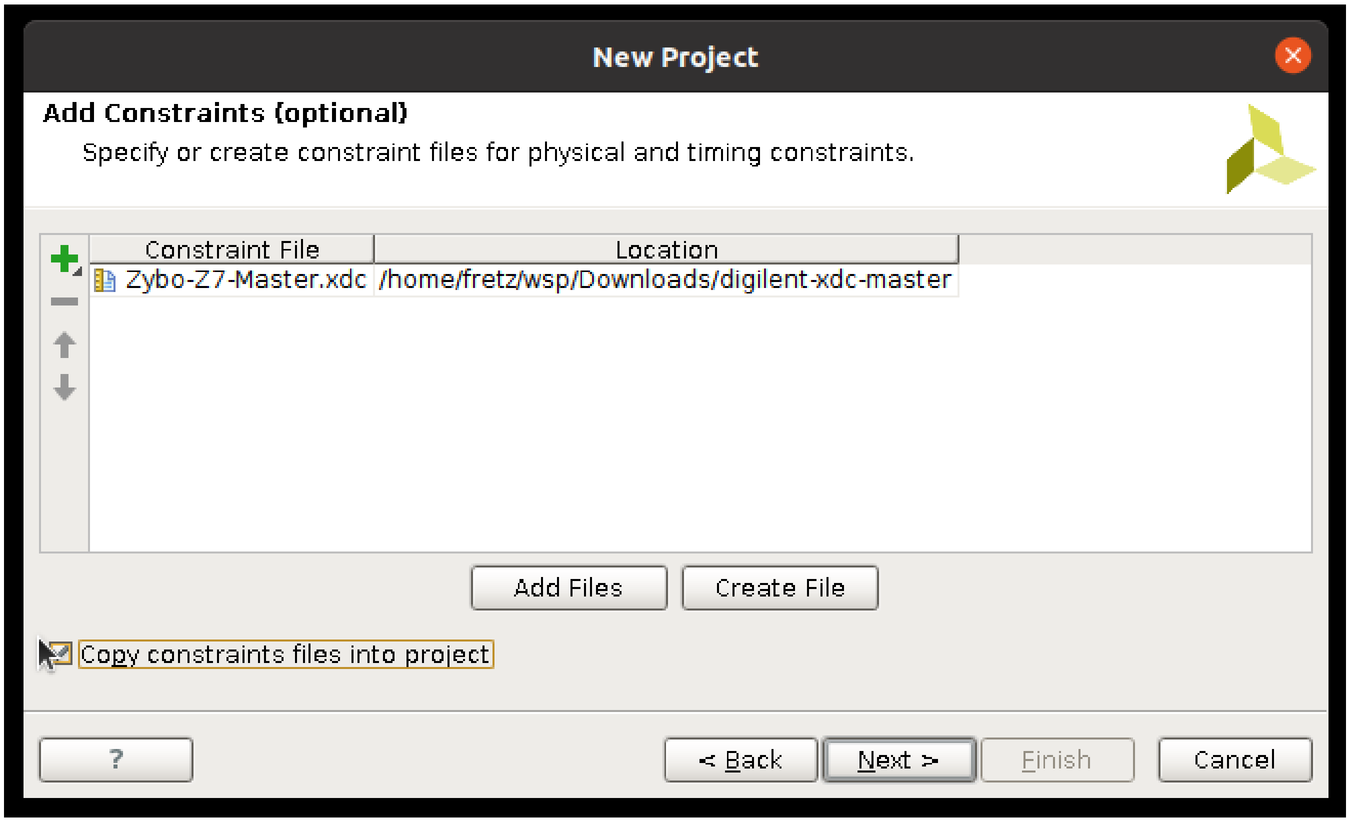
Arty-A7-35-Master.xdc
Arty-A7-100-Master.xdc
Arty-Master.xdc
Arty-S7-25-Master.xdc
Arty-S7-50-Master.xdc
Arty-Z7-10-Master.xdc
Arty-Z7-20-Master.xdc
Basys-3-Master.xdc
Cmod-A7-Master.xdc
Cmod-S7-25-Master.xdc
Cora-Z7-07S-Master.xdc
Cora-Z7-10-Master.xdc
Eclypse-Z7-Master.xdc
Genesys-2-Master.xdc
Genesys-ZU-3EG-D-Master.xdc
Genesys-ZU-3EG-Master.xdc
Genesys-ZU-5EV-D-Master.xdc
License.txt
Nexys-4-DDR-Master.xdc
Nexys-4-Master.xdc
Nexys-A7-50T-Master.xdc
Nexys-A7-100T-Master.xdc
Nexys-Video-Master.xdc
README.md
Sword-Master.xdc
USB104-A7-100T-Master.xdc
Zedboard-Master.xdc
Zybo-Master.xdc
Zybo-Z7-Master.xdc

/home/fretz/wsp/neorv32/rtl/test_setups

```
## This file is a general .xdc for the Zybo Z7 Rev. B
## It is compatible with the Zybo Z7-20 and Zybo Z7-10
## To use it in a project:
## - uncomment the lines corresponding to used pins
## - rename the used ports (in each line, after get_por

##Clock signal
#set_property -dict { PACKAGE_PIN K17   IOSTANDARD LVCM
#create_clock -add -name sys_clk_pin -period 8.00 -wave


##Switches
#set_property -dict { PACKAGE_PIN G15   IOSTANDARD LVCM
#set_property -dict { PACKAGE_PIN P15   IOSTANDARD LVCM
#set_property -dict { PACKAGE_PIN W13   IOSTANDARD LVCM
#set_property -dict { PACKAGE_PIN T16   IOSTANDARD LVCM


##Buttons
#set_property -dict { PACKAGE_PIN K18   IOSTANDARD LVCM
#set_property -dict { PACKAGE_PIN P16   IOSTANDARD LVCM
#set_property -dict { PACKAGE_PIN K19   IOSTANDARD LVCM
#set_property -dict { PACKAGE_PIN Y16   IOSTANDARD LVCM
```

File name: Zybo-Z7-Master.xdc
Files of type: All Files

- Tick the `copy constraints files into project` and click the Next button



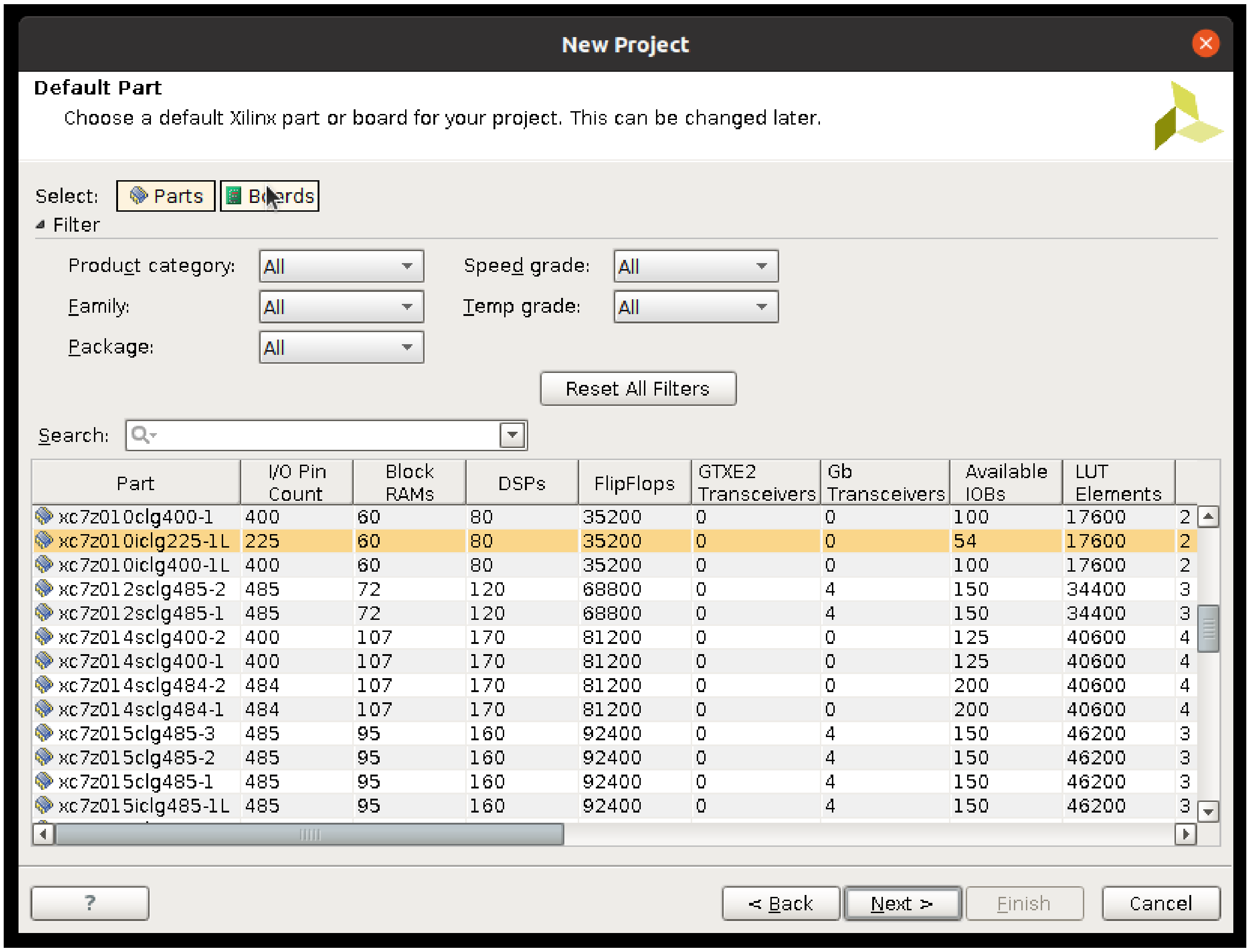
New Project

Add Constraints (optional)

Specify or create constraint files for physical and timing constraints.

Constraint File	Location
Zybo-Z7-Master.xdc	/home/fretz/wsp/Downloads/digilent-xdc-master

- Click on Boards


New Project

Default Part

Choose a default Xilinx part or board for your project. This can be changed later.

Select: Parts Boards

Filter

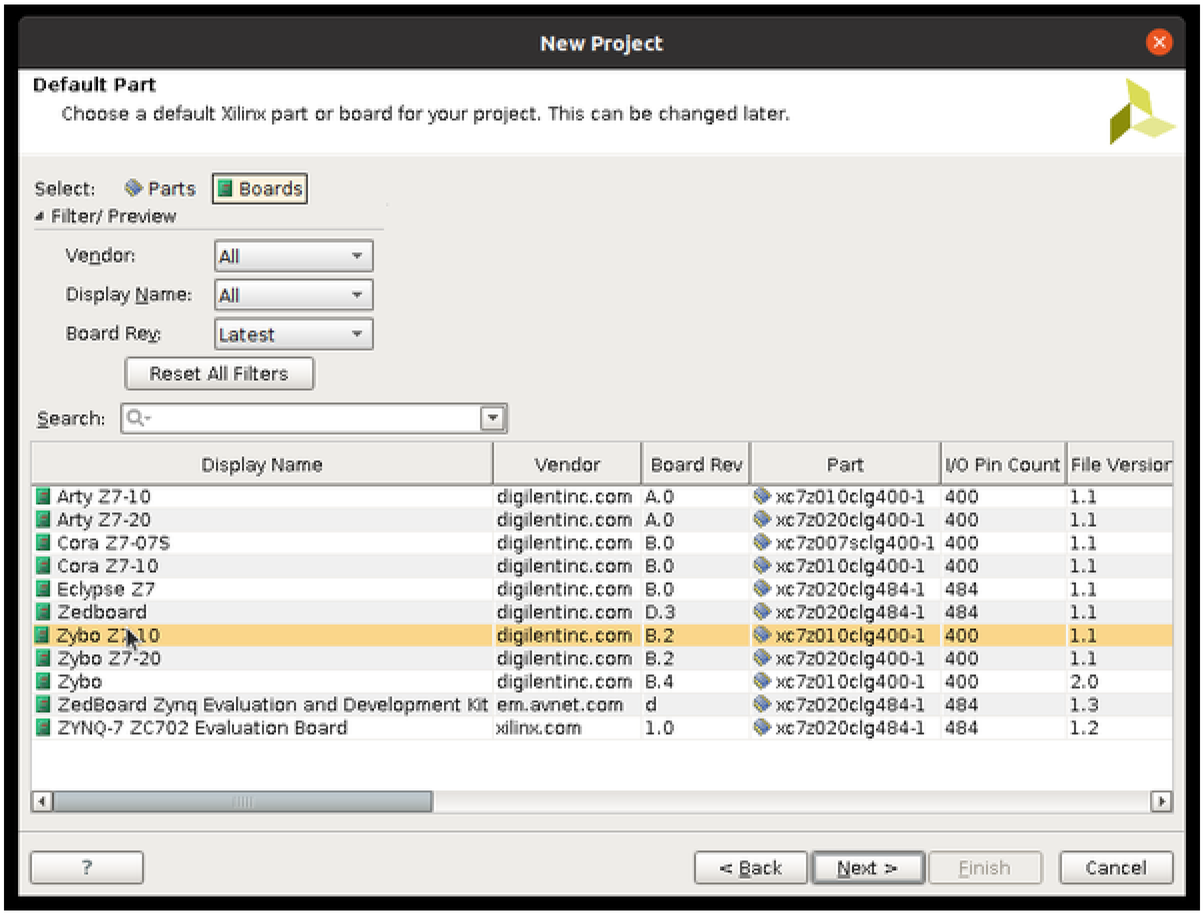
Product category: All
Speed grade: All
Family: All
Temp grade: All
Package: All

Reset All Filters

Search:

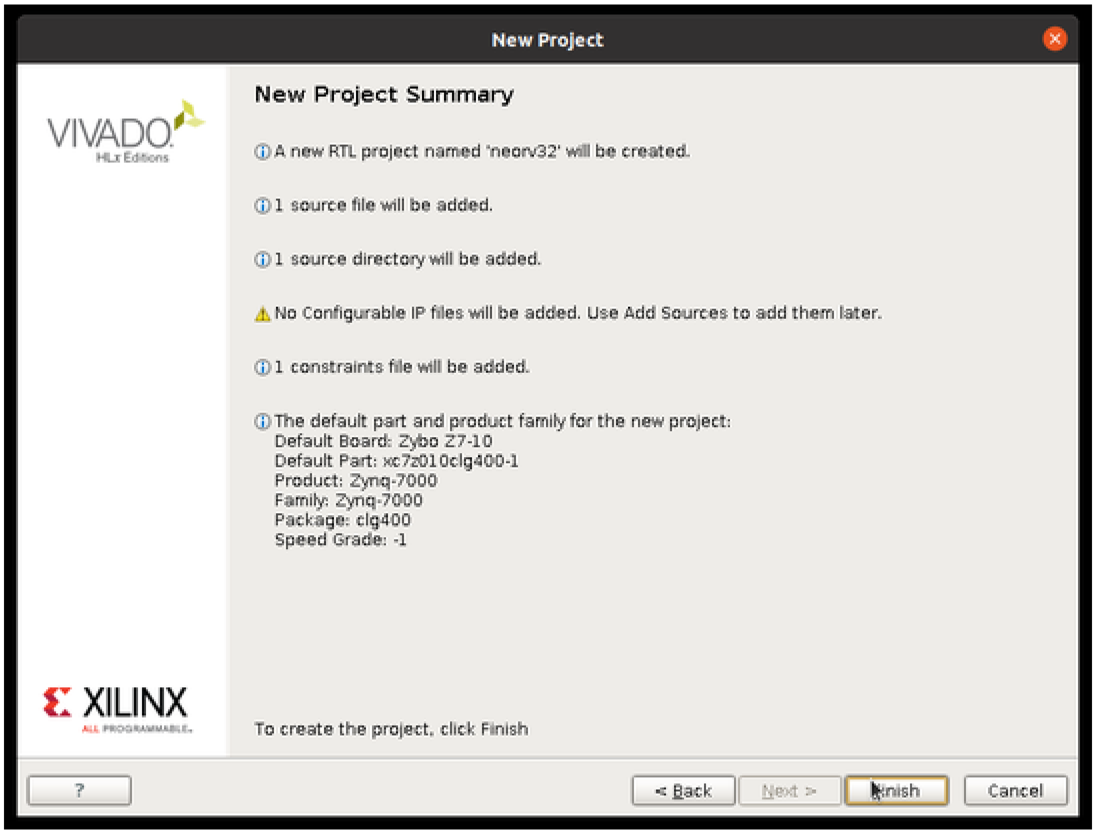
Part	I/O Pin Count	Block RAMs	DSPs	FlipFlops	GTXE2 Transceivers	Gb Transceivers	Available IOBs	LUT Elements	
xc7z010clg400-1	400	60	80	35200	0	0	100	17600	2
xc7z010iclg225-1L	225	60	80	35200	0	0	54	17600	2
xc7z010iclg400-1L	400	60	80	35200	0	0	100	17600	2
xc7z012sclg485-2	485	72	120	68800	0	4	150	34400	3
xc7z012sclg485-1	485	72	120	68800	0	4	150	34400	3
xc7z014sclg400-2	400	107	170	81200	0	0	125	40600	4
xc7z014sclg400-1	400	107	170	81200	0	0	125	40600	4
xc7z014sclg484-2	484	107	170	81200	0	0	200	40600	4
xc7z014sclg484-1	484	107	170	81200	0	0	200	40600	4
xc7z015clg485-3	485	95	160	92400	0	4	150	46200	3
xc7z015clg485-2	485	95	160	92400	0	4	150	46200	3
xc7z015clg485-1	485	95	160	92400	0	4	150	46200	3
xc7z015iclg485-1L	485	95	160	92400	0	4	150	46200	3

- Choose Zybo `Z7-10` and press the next button



Display Name	Vendor	Board Rev	Part	I/O Pin Count	File Version
Arty Z7-10	digilentinc.com	A.0	xc7z010clg400-1	400	1.1
Arty Z7-20	digilentinc.com	A.0	xc7z020clg400-1	400	1.1
Cora Z7-07S	digilentinc.com	B.0	xc7z007sclg400-1	400	1.1
Cora Z7-10	digilentinc.com	B.0	xc7z010clg400-1	400	1.1
Eclypse Z7	digilentinc.com	B.0	xc7z020clg484-1	484	1.1
Zedboard	digilentinc.com	D.3	xc7z020clg484-1	484	1.1
Zybo Z7-10	digilentinc.com	B.2	xc7z010clg400-1	400	1.1
Zybo Z7-20	digilentinc.com	B.2	xc7z020clg400-1	400	1.1
Zybo	digilentinc.com	B.4	xc7z010clg400-1	400	2.0
ZedBoard Zynq Evaluation and Development Kit	em.avnet.com	d	xc7z020clg484-1	484	1.3
ZYNQ-7 ZC702 Evaluation Board	xilinx.com	1.0	xc7z020clg484-1	484	1.2

- Finally, click on the Finish button



New Project Summary

ⓘ A new RTL project named 'neorv32' will be created.

ⓘ 1 source file will be added.

ⓘ 1 source directory will be added.

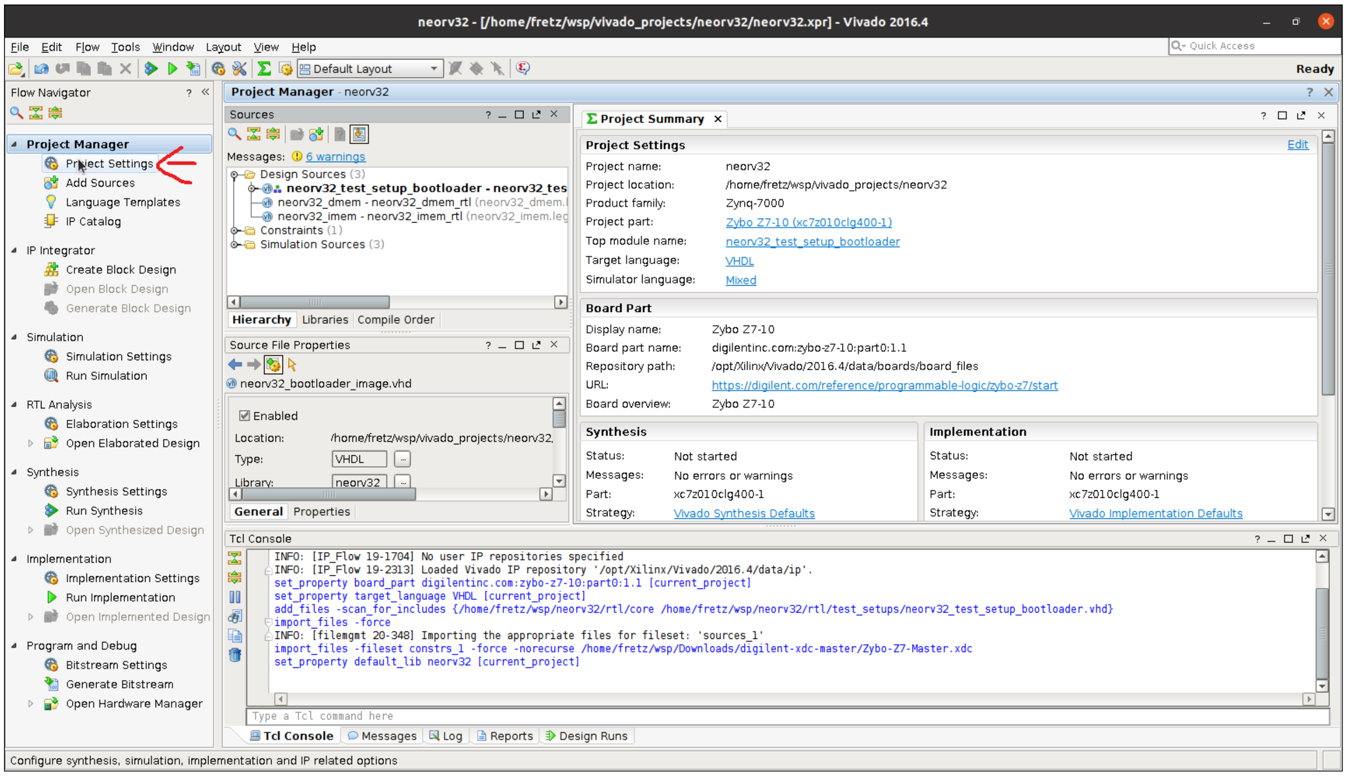
⚠ No Configurable IP files will be added. Use Add Sources to add them later.

ⓘ 1 constraints file will be added.

ⓘ The default part and product family for the new project:
Default Board: Zybo Z7-10
Default Part: xc7z010clg400-1
Product: Zynq-7000
Family: Zynq-7000
Package: clg400
Speed Grade: -1

To create the project, click Finish

- Select the Project Settings under the Project Manager



Project Settings

Project name:	neorv32
Project location:	/home/fretz/wsp/vivado_projects/neorv32
Product family:	Zynq-7000
Project part:	Zybo Z7-10 (xc7z010clg400-1)
Top module name:	neorv32_test_setup_bootloader
Target language:	VHDL
Simulator language:	Mixed

Board Part

Display name:	Zybo Z7-10
Board part name:	digilentinc.com:zybo-z7-10:part0:1.1
Repository path:	/opt/Xilinx/Vivado/2016.4/data/boards/board_files
URL:	https://digilent.com/reference/programmable-logic/zybo-z7/start
Board overview:	Zybo Z7-10

Synthesis

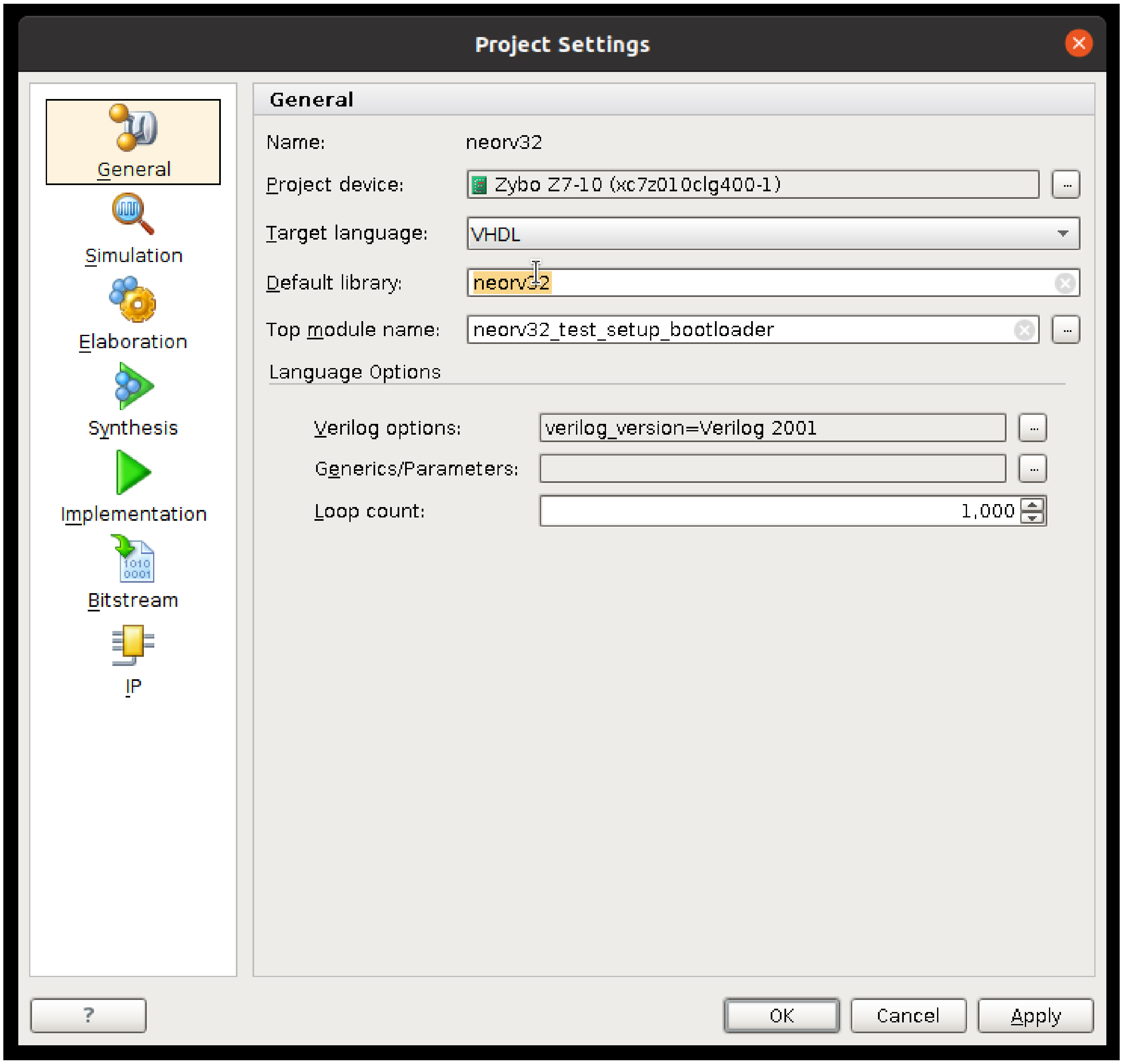
Status:	Not started
Messages:	No errors or warnings
Part:	xc7z010clg400-1
Strategy:	Vivado Synthesis Defaults

Implementation

Status:	Not started
Messages:	No errors or warnings
Part:	xc7z010clg400-1
Strategy:	Vivado Implementation Defaults

```
INFO: [IP_Flow 19-1704] No user IP repositories specified
INFO: [IP_Flow 19-2313] Loaded Vivado IP repository '/opt/Xilinx/Vivado/2016.4/data/ip'.
set_property board_part digilentinc.com:zybo-z7-10:part0:1.1 [current_project]
set_property target_language VHDL [current_project]
add_files -scan_for_includes {/home/fretz/wsp/neorv32/rtl/core /home/fretz/wsp/neorv32/rtl/test_setups/neorv32_test_setup_bootloader.vhd}
import_files -force
INFO: [filemgmt 20-348] Importing the appropriate files for fileset: 'sources_1'
import_files -fileset constrs_1 -force -norecurse /home/fretz/wsp/Downloads/digilent-xdc-master/Zybo-Z7-Master.xdc
set_property default_lib neorv32 [current_project]
```

- Rename the Default library `xil_defaultlib` with `neorv32`. Close the Project Settings by pressing the Apply and OK buttons



General

Name: neorv32

Project device: Zybo Z7-10 (xc7z010clg400-1)

Target language: VHDL

Default library: neorv32

Top module name: neorv32_test_setup_bootloader

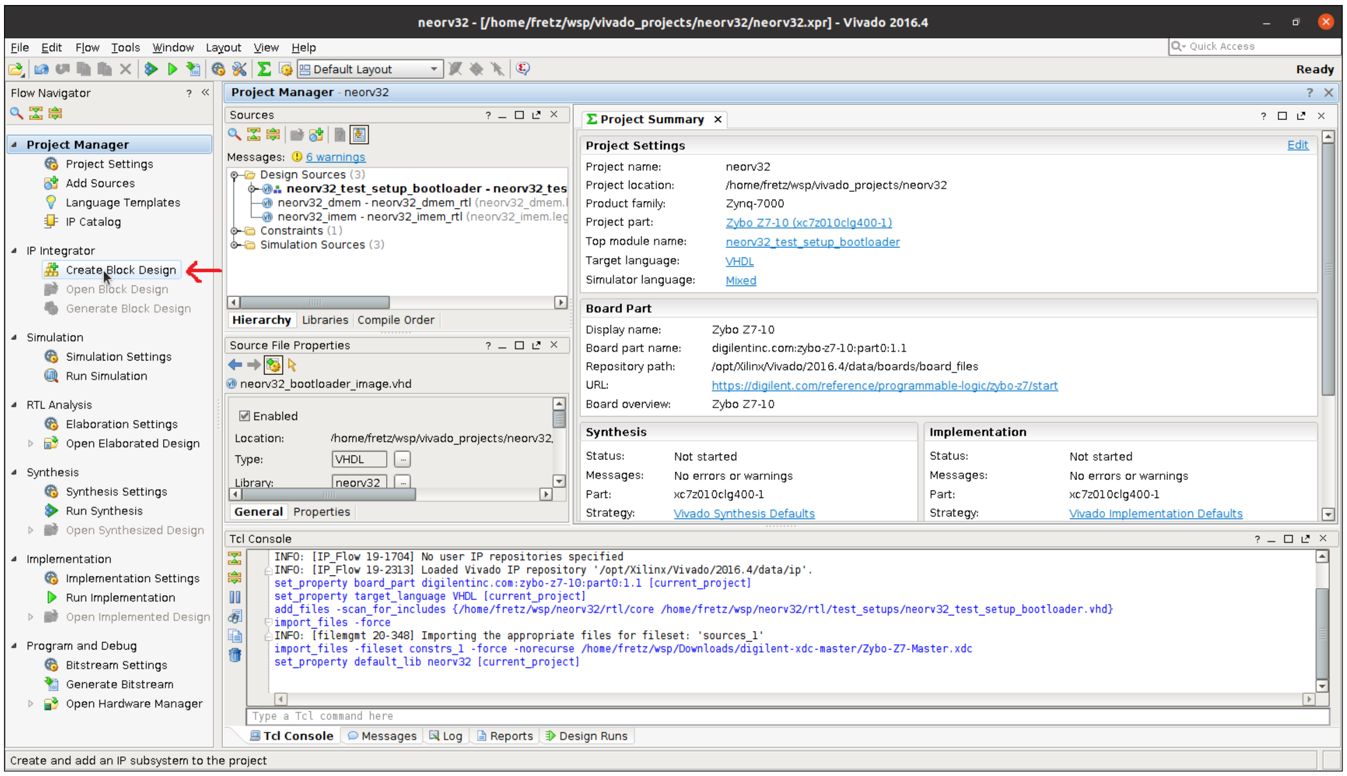
Language Options

Verilog options: verilog_version=Verilog 2001

Generics/Parameters:

Loop count: 1,000

- Click on the Create Block Design



Messages: 6 warnings

- Design Sources (3)
  - neorv32_test_setup_bootloader - neorv32_tes
    - neorv32_dmem - neorv32_dmem_rtl (neorv32_dmem.
    - neorv32_imem - neorv32_imem_rtl (neorv32_imem.leg
- Constraints (1)
- Simulation Sources (3)

neorv32_bootloader_image.vhd

Enabled

Location:	/home/fretz/wsp/vivado_projects/neorv32
Type:	VHDL
Library:	neorv32

Project Settings

Project name:	neorv32
Project location:	/home/fretz/wsp/vivado_projects/neorv32
Product family:	Zynq-7000
Project part:	Zybo Z7-10 (xc7z010clg400-1)
Top module name:	neorv32_test_setup_bootloader
Target language:	VHDL
Simulator language:	Mixed

Board Part

Display name:	Zybo Z7-10
Board part name:	digilentinc.com:zybo-z7-10:part0:1.1
Repository path:	/opt/Xilinx/Vivado/2016.4/data/boards/board_files
URL:	https://digilent.com/reference/programmable-logic/zybo-z7/start
Board overview:	Zybo Z7-10

Synthesis

Status:	Not started
Messages:	No errors or warnings
Part:	xc7z010clg400-1
Strategy:	Vivado Synthesis Defaults

Implementation

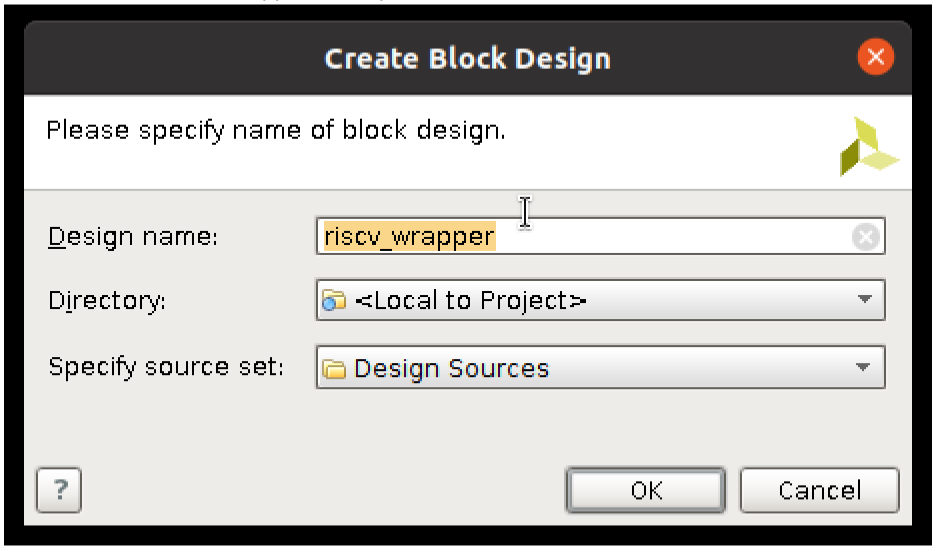
Status:	Not started
Messages:	No errors or warnings
Part:	xc7z010clg400-1
Strategy:	Vivado Implementation Defaults

```
INFO: [IP_Flow 19-1704] No user IP repositories specified
INFO: [IP_Flow 19-2313] Loaded Vivado IP repository '/opt/Xilinx/Vivado/2016.4/data/ip'.
set_property board_part digilentinc.com:zybo-z7-10:part0:1.1 [current_project]
set_property target_language VHDL [current_project]
add_files -scan_for_includes {/home/fretz/wsp/neorv32/rtl/core /home/fretz/wsp/neorv32/rtl/test_setups/neorv32_test_setup_bootloader.vhd}
import_files -force
INFO: [filemgmt 20-348] Importing the appropriate files for fileset: 'sources_1'
import_files -fileset constrs_1 -force -norecurse /home/fretz/wsp/Downloads/digilent-xdc-master/Zybo-Z7-Master.xdc
set_property default_lib neorv32 [current_project]
```

Type a Tcl command here

Create and add an IP subsystem to the project

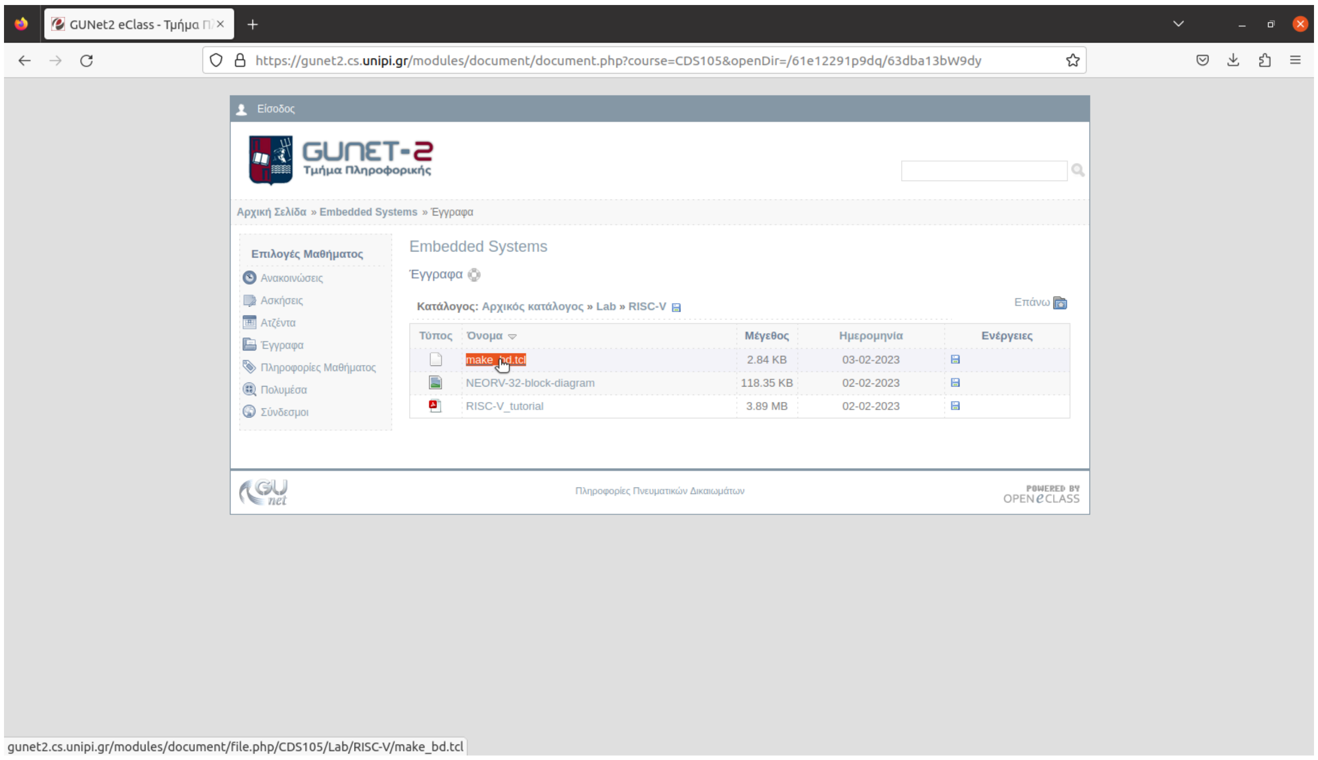
- Give the name `riscv_wrapper`. Then press the OK button



Please specify name of block design.

Design name:	riscv_wrapper
Directory:	<Local to Project>
Specify source set:	Design Sources

- Download the make_bd.tcl script from GUNET2
  - https://gunet2.cs.unipi.gr/modules/document/document.php?course=CDS105&openDir=/61e12291p9dq/63dba13bW9dy


GUNet2 eClass - Τμήμα Π

https://gunet2.cs.unipi.gr/modules/document/document.php?course=CDS105&openDir=/61e12291p9dq/63dba13bW9dy

Είσοδος

GUNET-2 Τμήμα Πληροφορικής

Αρχική Σελίδα » Embedded Systems » Έγγραφα

Επιλογές Μαθήματος: Ανακοινώσεις, Ασκήσεις, Ατζέντα, Έγγραφα, Πληροφορίες Μαθήματος, Πολυμέσα, Σύνδεσμοι

Embedded Systems

Έγγραφα

Κατάλογος: Αρχικός κατάλογος » Lab » RISC-V

Επάνω

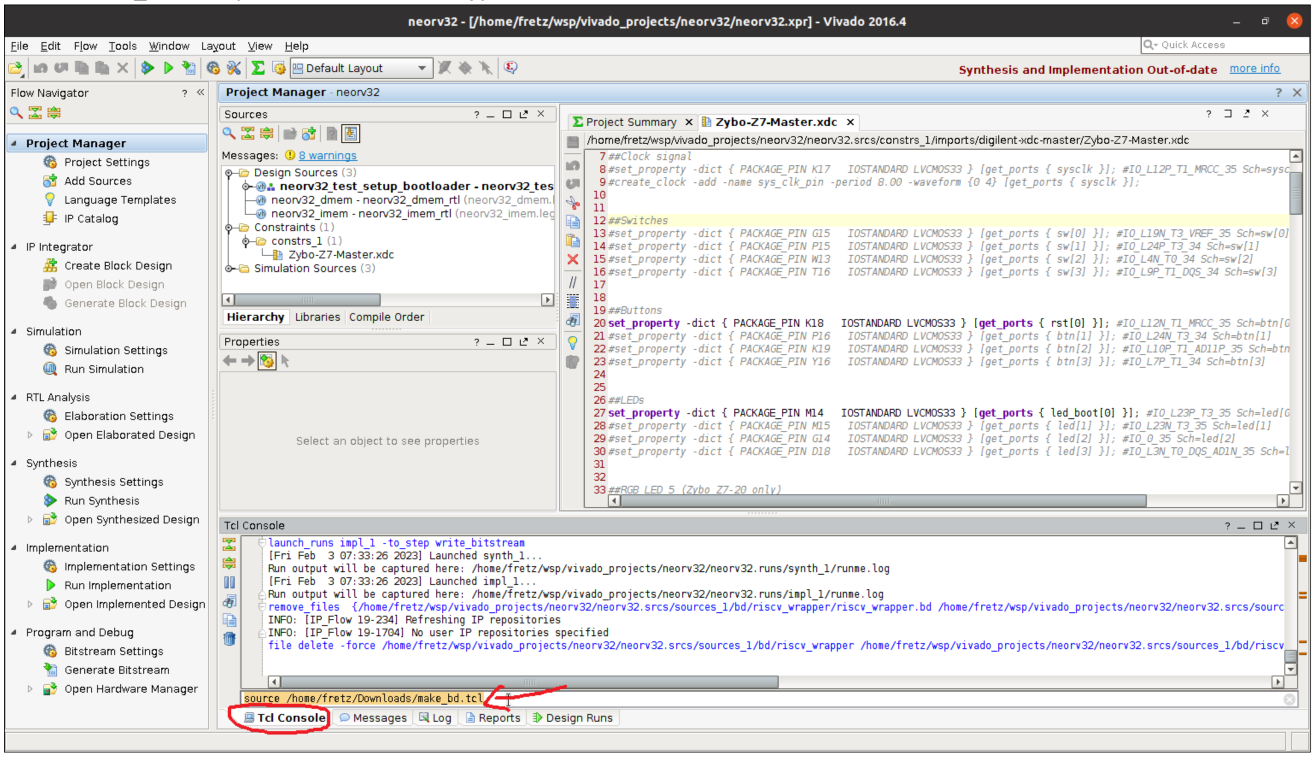
Τύπος	Όνομα	Μέγεθος	Ημερομηνία	Ενέργειες
	make_bd.tcl	2.84 KB	03-02-2023	
	NEORV-32-block-diagram	118.35 KB	02-02-2023	
	RISC-V_tutorial	3.89 MB	02-02-2023	

Πληροφορίες Πνευματικών Δικαιωμάτων

POWERED BY OPEN eCLASS

gunet2.cs.unipi.gr/modules/document/file.php/CDS105/Lab/RISC-V/make_bd.tcl

- Run the make_bd.tcl script from the tcl console. Type `source /home/fretz/Downloads/make_bd.tcl`


neorv32 - [/home/fretz/wsp/vivado_projects/neorv32/neorv32.xpr] - Vivado 2016.4

Synthesis and Implementation Out-of-date more info

Project Manager - neorv32

Sources

Messages: 8 warnings

```
Design Sources (3)
  neorv32_test_setup_bootloader - neorv32_tes
    neorv32_dmem - neorv32_dmem_rtl (neorv32_dmem.
    neorv32_imem - neorv32_imem_rtl (neorv32_imem.leg
Constraints (1)
  constrs_1 (1)
    Zybo-Z7-Master.xdc
Simulation Sources (3)
```

Select an object to see properties

Project Summary | Zybo-Z7-Master.xdc

/home/fretz/wsp/vivado_projects/neorv32/neorv32.srcs/constrs_1/imports/digilent-xdc-master/Zybo-Z7-Master.xdc

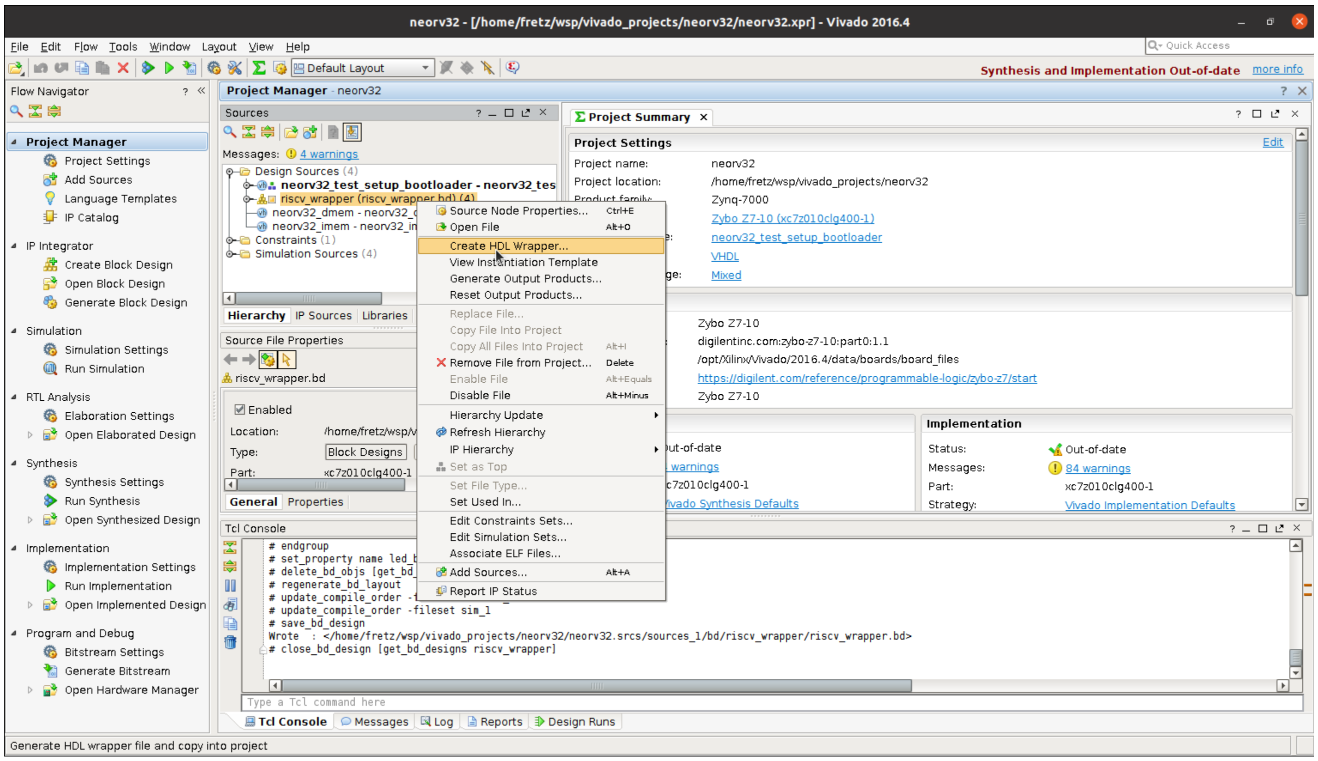
```
##Clock signal
#set_property -dict { PACKAGE_PIN K17   IOSTANDARD LVCMOS33 } [get_ports { sysclk }]; #IO_L12P_T1_MRCC_35 Sch=sysc
#create_clock -add -name sys_clk_pin -period 8.00 -waveform {0 4} [get_ports { sysclk }];


##Switches
#set_property -dict { PACKAGE_PIN G15   IOSTANDARD LVCMOS33 } [get_ports { sw[0] }]; #IO_L19N_T3_VREF_35 Sch=sw[0]
#set_property -dict { PACKAGE_PIN P15   IOSTANDARD LVCMOS33 } [get_ports { sw[1] }]; #IO_L24P_T3_34 Sch=sw[1]
#set_property -dict { PACKAGE_PIN W13   IOSTANDARD LVCMOS33 } [get_ports { sw[2] }]; #IO_L4N_T0_34 Sch=sw[2]
#set_property -dict { PACKAGE_PIN T16   IOSTANDARD LVCMOS33 } [get_ports { sw[3] }]; #IO_L9P_T1_DQS_34 Sch=sw[3]


##Buttons
set_property -dict { PACKAGE_PIN K18   IOSTANDARD LVCMOS33 } [get_ports { rst[0] }]; #IO_L12N_T1_MRCC_35 Sch=btn[0
#set_property -dict { PACKAGE_PIN P16   IOSTANDARD LVCMOS33 } [get_ports { btn[1] }]; #IO_L24N_T3_34 Sch=btn[1]
#set_property -dict { PACKAGE_PIN K19   IOSTANDARD LVCMOS33 } [get_ports { btn[2] }]; #IO_L10P_T1_AD11P_35 Sch=btn
#set_property -dict { PACKAGE_PIN Y16   IOSTANDARD LVCMOS33 } [get_ports { btn[3] }]; #IO_L7P_T1_34 Sch=btn[3]


##LEDs
set_property -dict { PACKAGE_PIN M14   IOSTANDARD LVCMOS33 } [get_ports { led_boot[0] }]; #IO_L23P_T3_35 Sch=led[0
#set_property -dict { PACKAGE_PIN M15   IOSTANDARD LVCMOS33 } [get_ports { led[1] }]; #IO_L23N_T3_35 Sch=led[1]
#set_property -dict { PACKAGE_PIN G14   IOSTANDARD LVCMOS33 } [get_ports { led[2] }]; #IO_0_35 Sch=led[2]
#set_property -dict { PACKAGE_PIN D18   IOSTANDARD LVCMOS33 } [get_ports { led[3] }]; #IO_L3N_T0_DQS_AD1N_35 Sch=l


##RGB LED 5 (Zybo Z7-20 only)
```

Tcl Console

```
launch_runs impl_1 -to_step write_bitstream
[Fri Feb  3 07:33:26 2023] Launched synth_1...
Run output will be captured here: /home/fretz/wsp/vivado_projects/neorv32/neorv32.runs/synth_1/runme.log
[Fri Feb  3 07:33:26 2023] Launched impl_1...
Run output will be captured here: /home/fretz/wsp/vivado_projects/neorv32/neorv32.runs/impl_1/runme.log
remove_files  {/home/fretz/wsp/vivado_projects/neorv32/neorv32.srcs/sources_1/bd/riscv_wrapper/riscv_wrapper.bd /home/fretz/wsp/vivado_projects/neorv32/neorv32.srcs/sourc
INFO: [IP_Flow 19-234] Refreshing IP repositories
INFO: [IP_Flow 19-1704] No user IP repositories specified
file delete -force /home/fretz/wsp/vivado_projects/neorv32/neorv32.srcs/sources_1/bd/riscv_wrapper /home/fretz/wsp/vivado_projects/neorv32/neorv32.srcs/sources_1/bd/riscv
```

```
source /home/fretz/Downloads/make_bd.tcl
```

- Next, create a VHDL wrapper for the block design



Sources

Messages: 4 warnings

- Design Sources (4)
  - neorv32_test_setup_bootloader - neorv32_tes
  - riscv_wrapper (riscv_wrapper.bd) (4)
    - neorv32_dmem - neorv32_c
    - neorv32_imem - neorv32_in
- Constraints (1)
- Simulation Sources (4)

Source File Properties

riscv_wrapper.bd

Enabled [✓]

Location:	/home/fretz/wsp/v
Type:	Block Designs
Part:	xc7z010clg400-1

Project Summary

Project Settings

Project name:	neorv32
Project location:	/home/fretz/wsp/vivado_projects/neorv32
Product family:	Zynq-7000
	Zybo Z7-10 (xc7z010clg400-1)
	neorv32_test_setup_bootloader
	VHDL
	Mixed

Zybo Z7-10
digilentinc.com:zybo-z7-10:part0:1.1
/opt/Xilinx/Vivado/2016.4/data/boards/board_files
https://digilent.com/reference/programmable-logic/zybo-z7/start
Zybo Z7-10

	ut-of-date
	warnings
	c7z010clg400-1
	ivado Synthesis Defaults

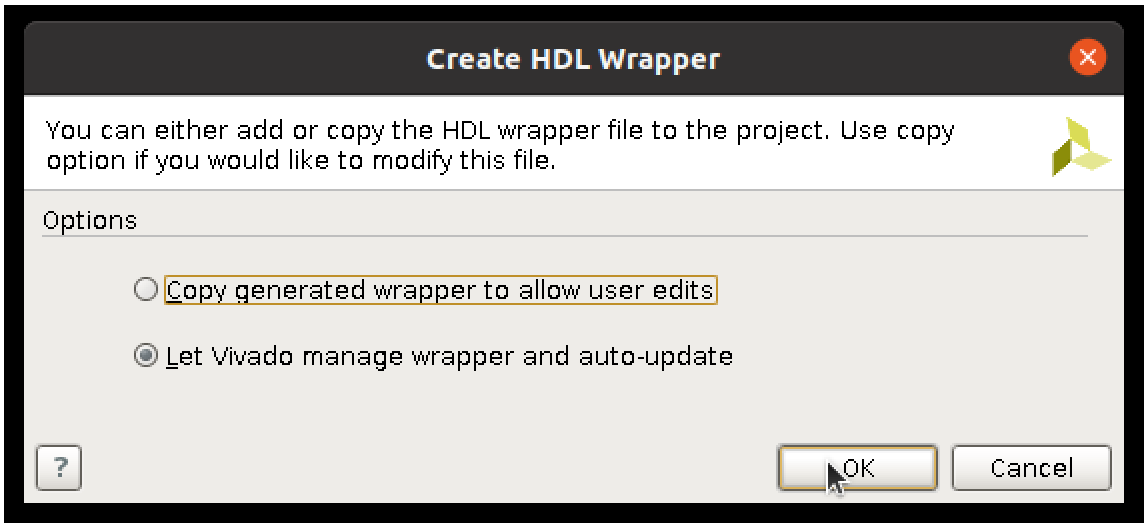
Implementation

Status:	Out-of-date
Messages:	84 warnings
Part:	xc7z010clg400-1
Strategy:	Vivado Implementation Defaults

```
# endgroup
# set_property name led_b
# delete_bd_objs [get_bd_
# regenerate_bd_layout
# update_compile_order -f
# update_compile_order -fileset sim_1
# save_bd_design
Wrote  : </home/fretz/wsp/vivado_projects/neorv32/neorv32.srcs/sources_1/bd/riscv_wrapper/riscv_wrapper.bd>
# close_bd_design [get_bd_designs riscv_wrapper]
```

Generate HDL wrapper file and copy into project

- Select the `Let Vivado manage` and click the OK button



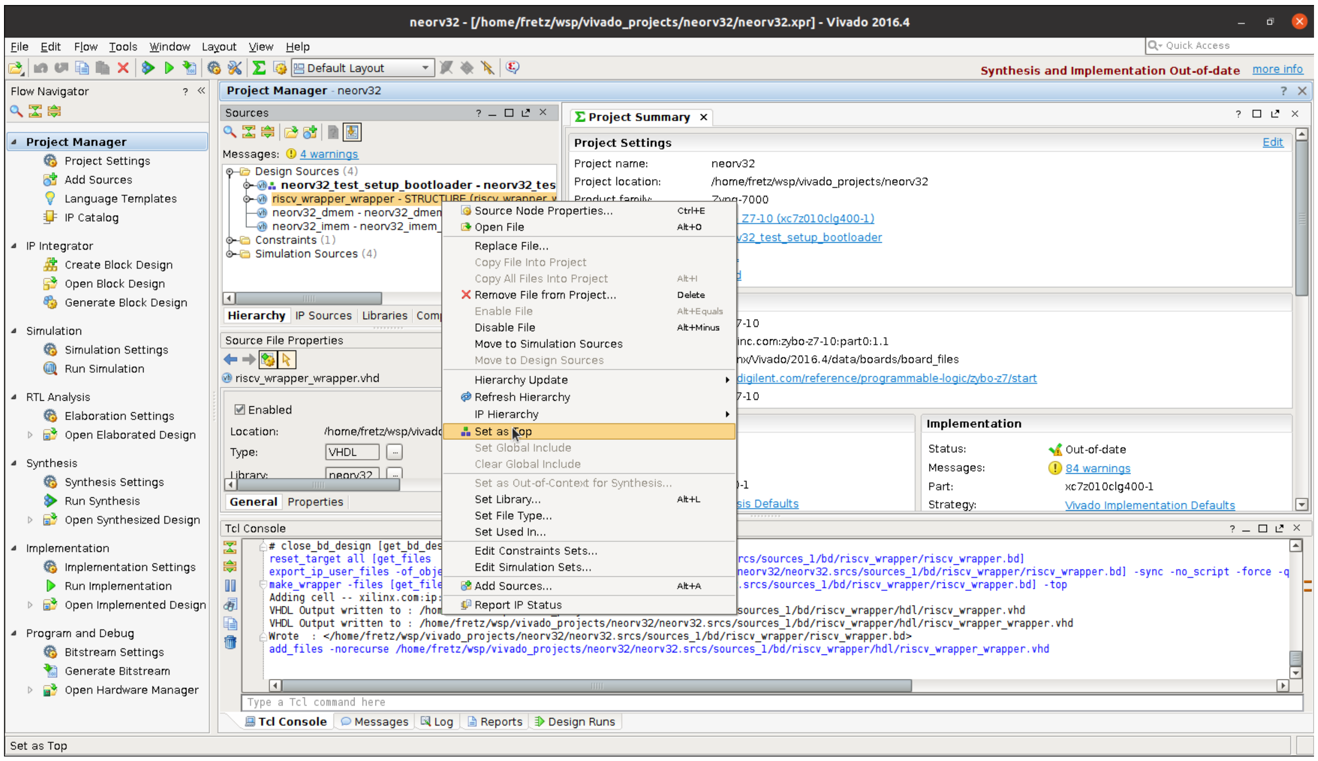
You can either add or copy the HDL wrapper file to the project. Use copy option if you would like to modify this file.

Options

( ) Copy generated wrapper to allow user edits

(●) Let Vivado manage wrapper and auto-update

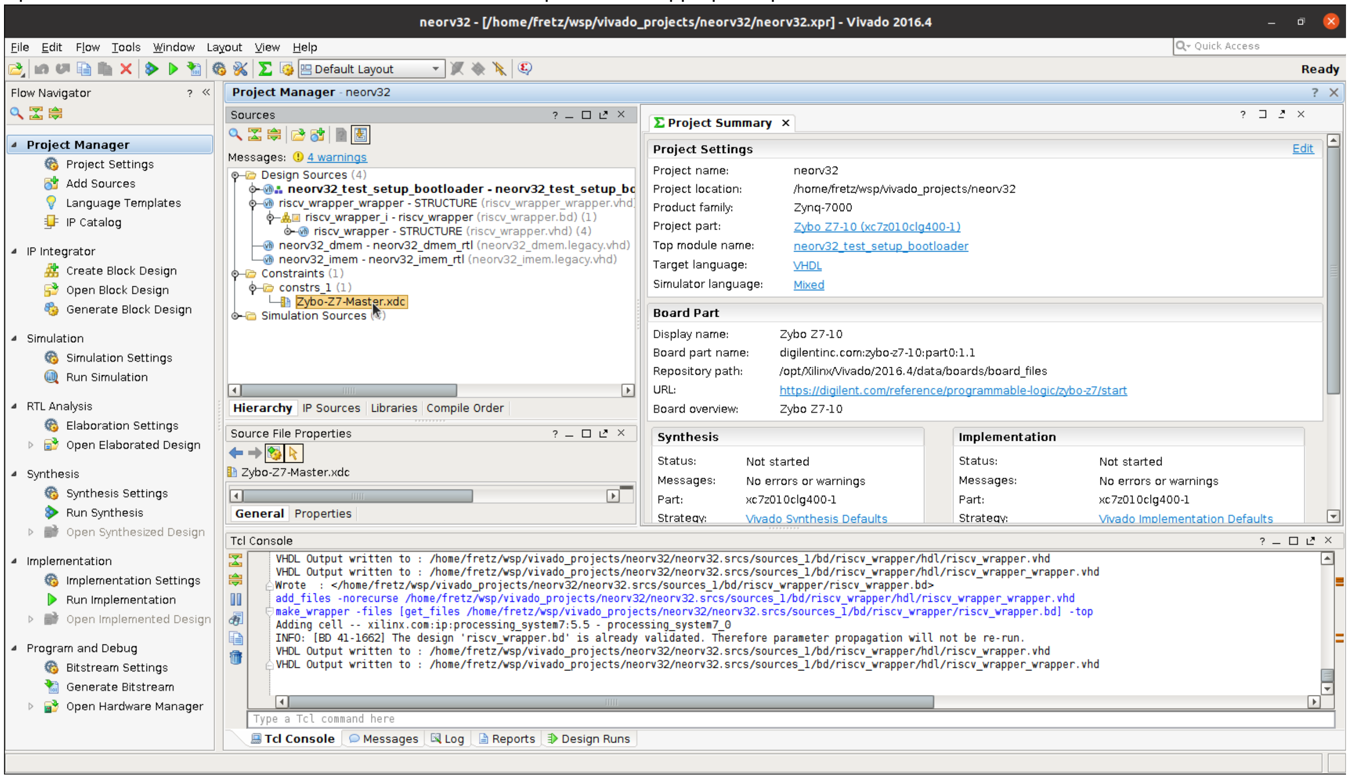
- Next, set as the top module the wrapper you just created



```
Design Sources (4)
  neorv32_test_setup_bootloader - neorv32_tes
  riscv_wrapper_wrapper - STRUCTURE (riscv_wrapper_w
  neorv32_dmem - neorv32_dmen
  neorv32_imem - neorv32_imem
Constraints (1)
Simulation Sources (4)
```

```
# close_bd_design [get_bd_des
reset_target all [get_files                                          rcs/sources_1/bd/riscv_wrapper/riscv_wrapper.bd]
export_ip_user_files -of_obje                                        neorv32/neorv32.srcs/sources_1/bd/riscv_wrapper/riscv_wrapper.bd] -sync -no_script -force -q
make_wrapper -files [get_file                                        .srcs/sources_1/bd/riscv_wrapper/riscv_wrapper.bd] -top
Adding cell -- xilinx.com:ip:
VHDL Output written to : /hom                                        sources_1/bd/riscv_wrapper/hdl/riscv_wrapper.vhd
VHDL Output written to : /home/fretz/wsp/vivado_projects/neorv32/neorv32.srcs/sources_1/bd/riscv_wrapper/hdl/riscv_wrapper_wrapper.vhd
Wrote  : </home/fretz/wsp/vivado_projects/neorv32/neorv32.srcs/sources_1/bd/riscv_wrapper/riscv_wrapper.bd>
add_files -norecurse /home/fretz/wsp/vivado_projects/neorv32/neorv32.srcs/sources_1/bd/riscv_wrapper/hdl/riscv_wrapper_wrapper.vhd
```

- Open the XDC file of the board to connect the NEORV32 ports to the appropriate pins of the FPGA.


neorv32 - [/home/fretz/wsp/vivado_projects/neorv32/neorv32.xpr] - Vivado 2016.4
Ready

```
Design Sources (4)
  neorv32_test_setup_bootloader - neorv32_test_setup_bc
  riscv_wrapper_wrapper - STRUCTURE (riscv_wrapper_wrapper.vhd)
    riscv_wrapper_i - riscv_wrapper (riscv_wrapper.bd) (1)
      riscv_wrapper - STRUCTURE (riscv_wrapper.vhd) (4)
  neorv32_dmem - neorv32_dmem_rtl (neorv32_dmem.legacy.vhd)
  neorv32_imem - neorv32_imem_rtl (neorv32_imem.legacy.vhd)
Constraints (1)
  constrs_1 (1)
    Zybo-Z7-Master.xdc
Simulation Sources (4)
```

Project Settings	
Project name:	neorv32
Project location:	/home/fretz/wsp/vivado_projects/neorv32
Product family:	Zynq-7000
Project part:	Zybo Z7-10 (xc7z010clg400-1)
Top module name:	neorv32_test_setup_bootloader
Target language:	VHDL
Simulator language:	Mixed

Board Part	
Display name:	Zybo Z7-10
Board part name:	digilentinc.com:zybo-z7-10:part0:1.1
Repository path:	/opt/Xilinx/Vivado/2016.4/data/boards/board_files
URL:	https://digilent.com/reference/programmable-logic/zybo-z7/start
Board overview:	Zybo Z7-10

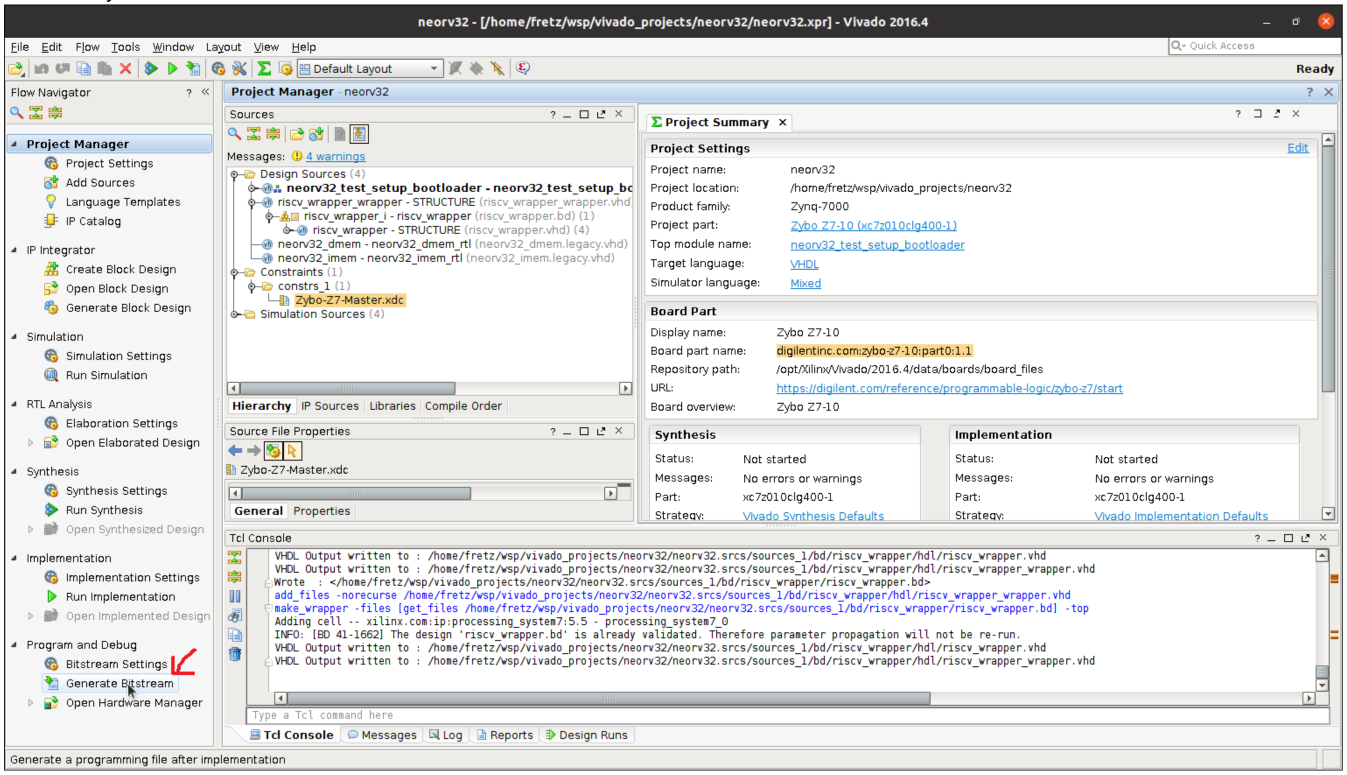
Synthesis		Implementation	
Status:	Not started	Status:	Not started
Messages:	No errors or warnings	Messages:	No errors or warnings
Part:	xc7z010clg400-1	Part:	xc7z010clg400-1
Strategy:	Vivado Synthesis Defaults	Strategy:	Vivado Implementation Defaults

```
VHDL Output written to : /home/fretz/wsp/vivado_projects/neorv32/neorv32.srcs/sources_1/bd/riscv_wrapper/hdl/riscv_wrapper.vhd
VHDL Output written to : /home/fretz/wsp/vivado_projects/neorv32/neorv32.srcs/sources_1/bd/riscv_wrapper/hdl/riscv_wrapper_wrapper.vhd
Wrote  : </home/fretz/wsp/vivado_projects/neorv32/neorv32.srcs/sources_1/bd/riscv_wrapper/riscv_wrapper.bd>
add_files -norecurse /home/fretz/wsp/vivado_projects/neorv32/neorv32.srcs/sources_1/bd/riscv_wrapper/hdl/riscv_wrapper_wrapper.vhd
make_wrapper -files [get_files /home/fretz/wsp/vivado_projects/neorv32/neorv32.srcs/sources_1/bd/riscv_wrapper/riscv_wrapper.bd] -top
Adding cell -- xilinx.com:ip:processing_system7:5.5 - processing_system7_0
INFO: [BD 41-1662] The design 'riscv_wrapper.bd' is already validated. Therefore parameter propagation will not be re-run.
VHDL Output written to : /home/fretz/wsp/vivado_projects/neorv32/neorv32.srcs/sources_1/bd/riscv_wrapper/hdl/riscv_wrapper.vhd
VHDL Output written to : /home/fretz/wsp/vivado_projects/neorv32/neorv32.srcs/sources_1/bd/riscv_wrapper/hdl/riscv_wrapper_wrapper.vhd
```

- You should modify the following pins

```
## RISC-V Reset
set_property -dict { PACKAGE_PIN K18   IOSTANDARD LVCMOS33 }
[get_ports { rst[0] }]; #IO_L12N_T1_MRCC_35 Sch=btn[0]
# RISC-V LEDs
set_property -dict { PACKAGE_PIN M14   IOSTANDARD LVCMOS33 }
[get_ports { led_boot[0] }]; #IO_L23P_T3_35 Sch=led[0]
##Pmod Header JC
set_property -dict { PACKAGE_PIN V15   IOSTANDARD LVCMOS33 }
[get_ports { uart_rxd }]; #IO_L10P_T1_34 Sch=JC1_P
set_property -dict { PACKAGE_PIN W15   IOSTANDARD LVCMOS33 }
[get_ports { uart_txd }]; #IO_L10N_T1_34 Sch=JC1_N
```

- Save the XDC file and press the Generate Bitstream button. This will generate the bitstream after synthesis and implementation are successfully finished.



Project Settings

Project name:	neorv32
Project location:	/home/fretz/wsp/vivado_projects/neorv32
Product family:	Zynq-7000
Project part:	Zybo Z7-10 (xc7z010clg400-1)
Top module name:	neorv32_test_setup_bootloader
Target language:	VHDL
Simulator language:	Mixed

Board Part

Display name:	Zybo Z7-10
Board part name:	digilentinc.com:zybo-z7-10:part0:1.1
Repository path:	/opt/Xilinx/Vivado/2016.4/data/boards/board_files
URL:	https://digilent.com/reference/programmable-logic/zybo-z7/start
Board overview:	Zybo Z7-10

Synthesis

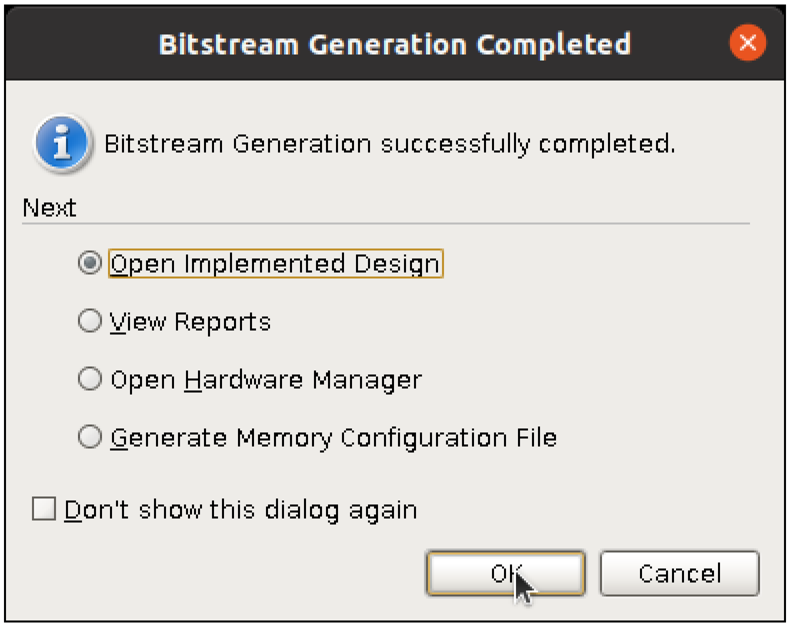
Status:	Not started
Messages:	No errors or warnings
Part:	xc7z010clg400-1
Strategy:	Vivado Synthesis Defaults

Implementation

Status:	Not started
Messages:	No errors or warnings
Part:	xc7z010clg400-1
Strategy:	Vivado Implementation Defaults

```
VHDL Output written to : /home/fretz/wsp/vivado_projects/neorv32/neorv32.srcs/sources_1/bd/riscv_wrapper/hdl/riscv_wrapper.vhd
VHDL Output written to : /home/fretz/wsp/vivado_projects/neorv32/neorv32.srcs/sources_1/bd/riscv_wrapper/hdl/riscv_wrapper_wrapper.vhd
Wrote  : </home/fretz/wsp/vivado_projects/neorv32/neorv32.srcs/sources_1/bd/riscv_wrapper/riscv_wrapper.bd>
add_files -norecurse /home/fretz/wsp/vivado_projects/neorv32/neorv32.srcs/sources_1/bd/riscv_wrapper/hdl/riscv_wrapper_wrapper.vhd
make_wrapper -files [get_files /home/fretz/wsp/vivado_projects/neorv32/neorv32.srcs/sources_1/bd/riscv_wrapper/riscv_wrapper.bd] -top
Adding cell -- xilinx.com:ip:processing_system7:5.5 - processing_system7_0
INFO: [BD 41-1662] The design 'riscv_wrapper.bd' is already validated. Therefore parameter propagation will not be re-run.
VHDL Output written to : /home/fretz/wsp/vivado_projects/neorv32/neorv32.srcs/sources_1/bd/riscv_wrapper/hdl/riscv_wrapper.vhd
VHDL Output written to : /home/fretz/wsp/vivado_projects/neorv32/neorv32.srcs/sources_1/bd/riscv_wrapper/hdl/riscv_wrapper_wrapper.vhd
```

- When the bitstream generation finishes, open to see the implemented design
-



Bitstream Generation Completed

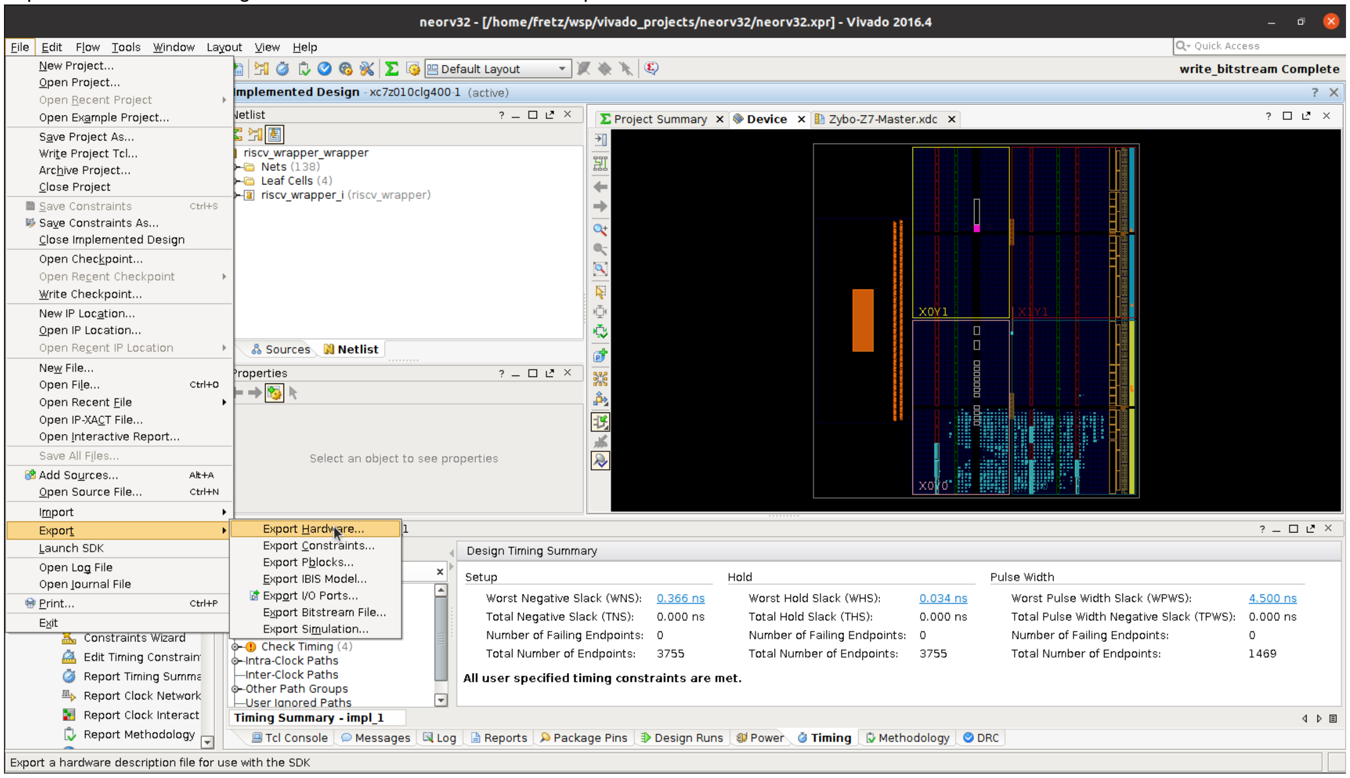
Bitstream Generation successfully completed.

Next

[✓ Open Implemented Design]
View Reports
Open Hardware Manager
Generate Memory Configuration File

Don't show this dialog again

- Export the hardware design to the Xilinx SDK software development framework



neorv32 - [/home/fretz/wsp/vivado_projects/neorv32/neorv32.xpr] - Vivado 2016.4

write_bitstream Complete

Implemented Design - xc7z010clg400-1 (active)

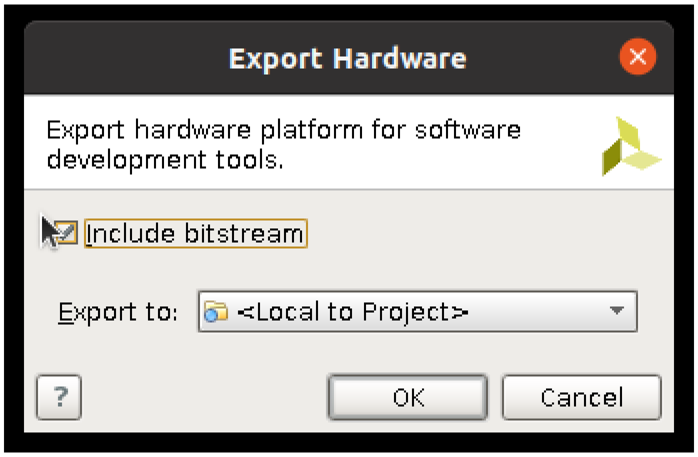
Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	0.366 ns	Worst Hold Slack (WHS):	0.034 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	3755	Total Number of Endpoints:	3755	Total Number of Endpoints:	1469

All user specified timing constraints are met.

Export a hardware description file for use with the SDK

- Click the Include bitstream and the OK button

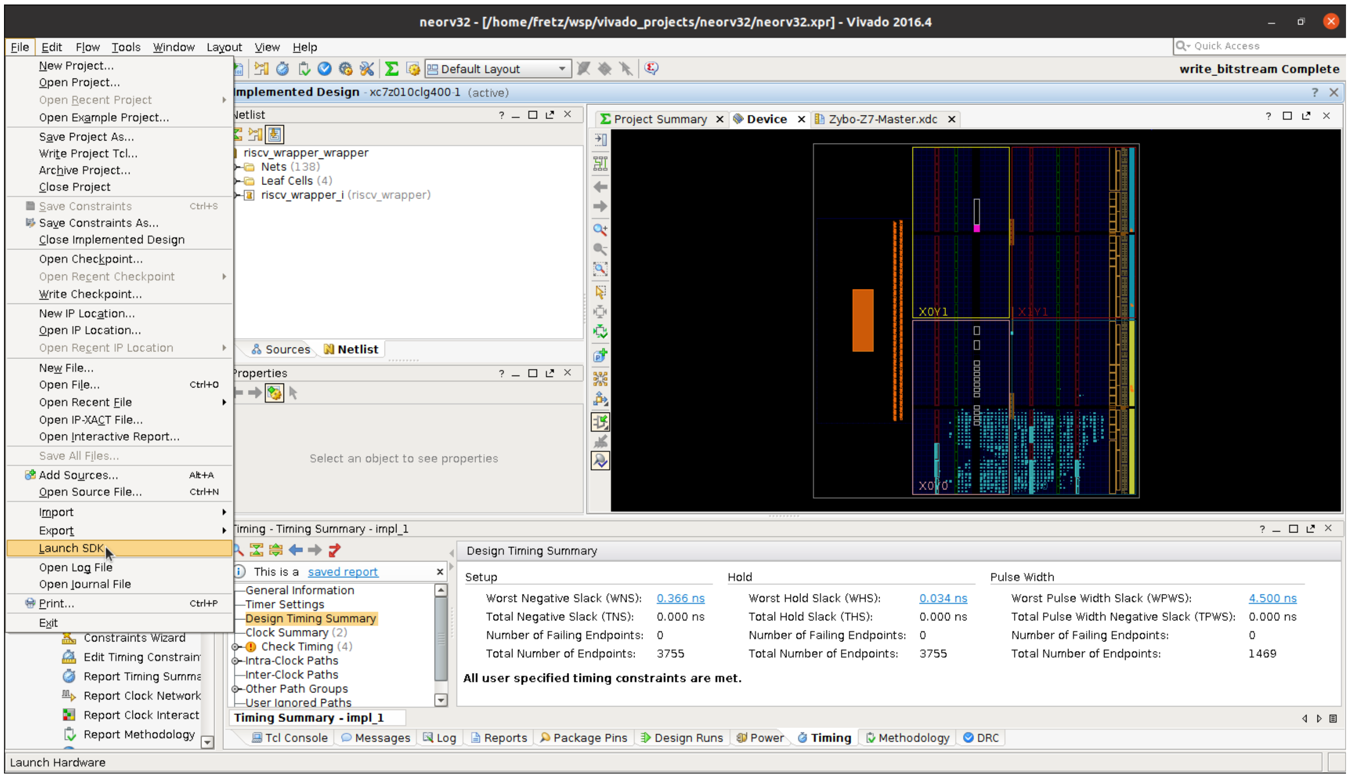


Export hardware platform for software development tools.

[✓] Include bitstream

Export to: <Local to Project>

- Lunch the SDK framework



neorv32 - [/home/fretz/wsp/vivado_projects/neorv32/neorv32.xpr] - Vivado 2016.4

write_bitstream Complete

Implemented Design - xc7z010clg400-1 (active)

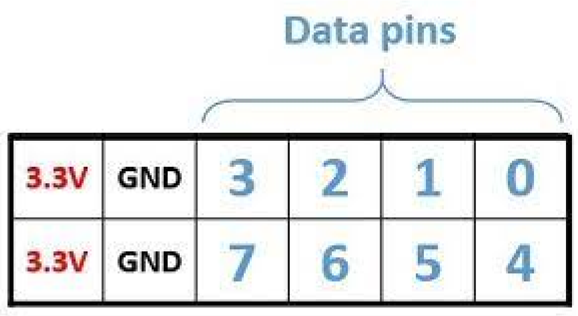
Design Timing Summary

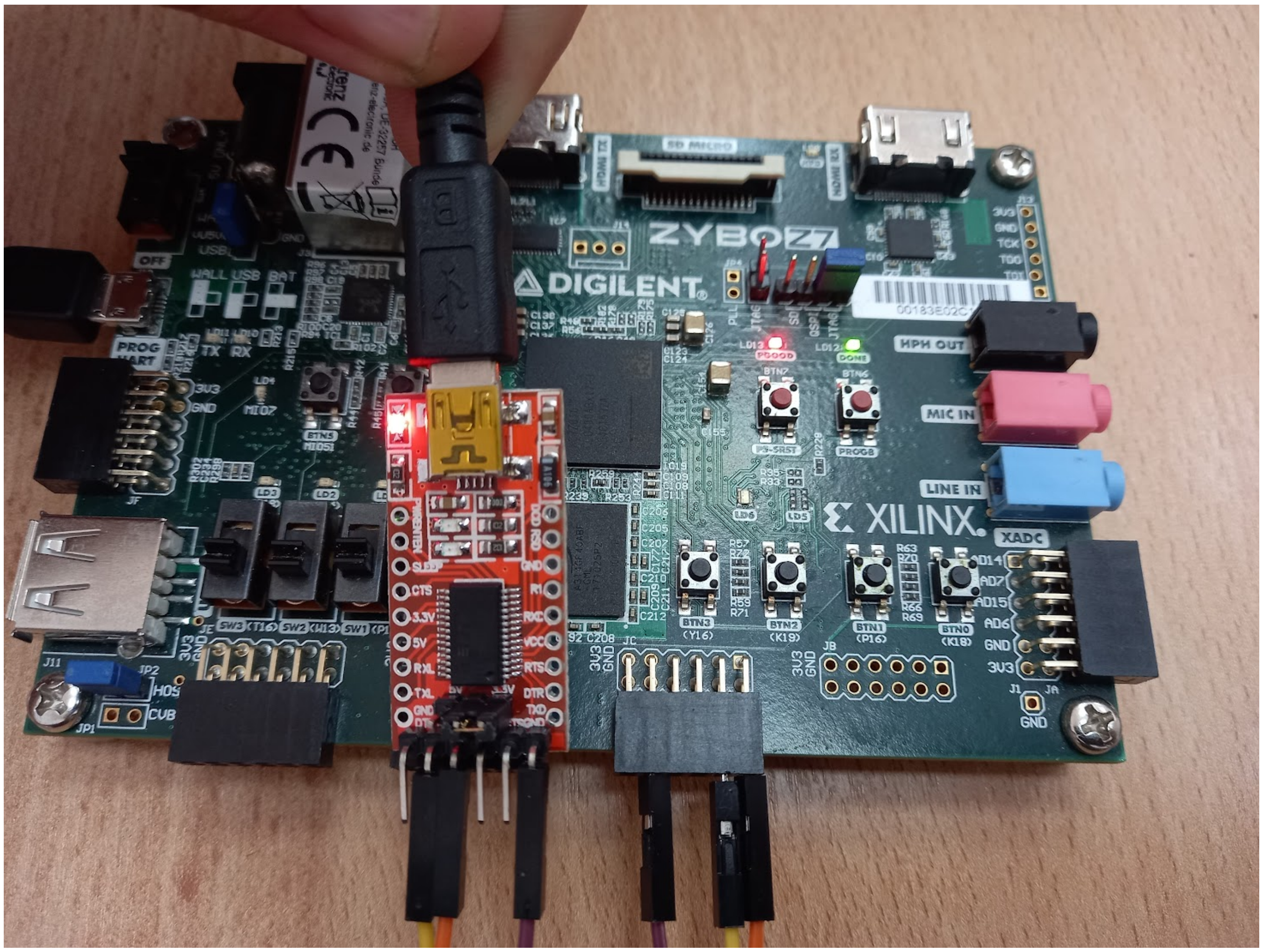
Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	0.366 ns	Worst Hold Slack (WHS):	0.034 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	3755	Total Number of Endpoints:	3755	Total Number of Endpoints:	1469

All user specified timing constraints are met.

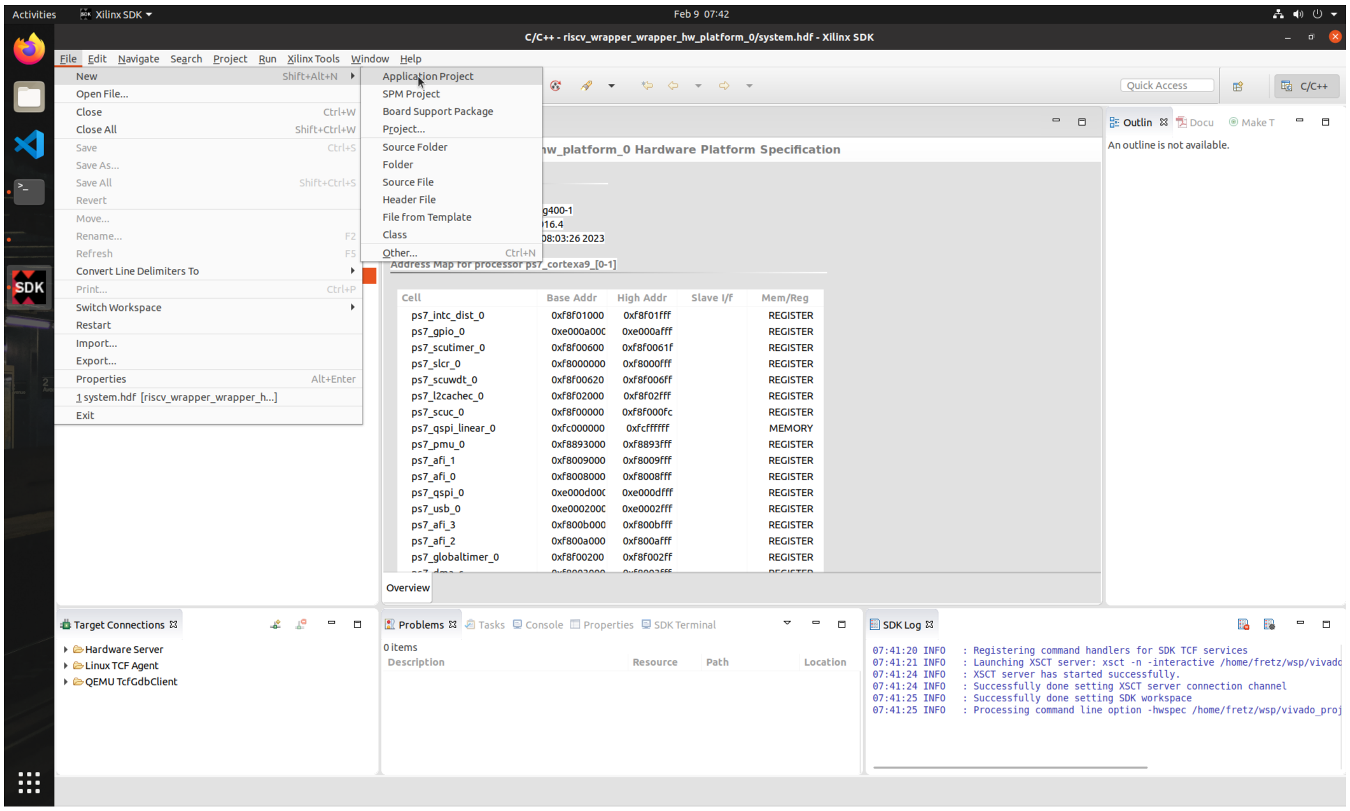
Board setup and run hello world software on the NEORV-32

- In order to get UART access on NEORV-32, we need to connect a USB/TTL UART external board on the PMOD header JC.





- In SDK, press: File New Application Project



C/C++ - riscv_wrapper_wrapper_hw_platform_0/system.hdf - Xilinx SDK

hw_platform_0 Hardware Platform Specification

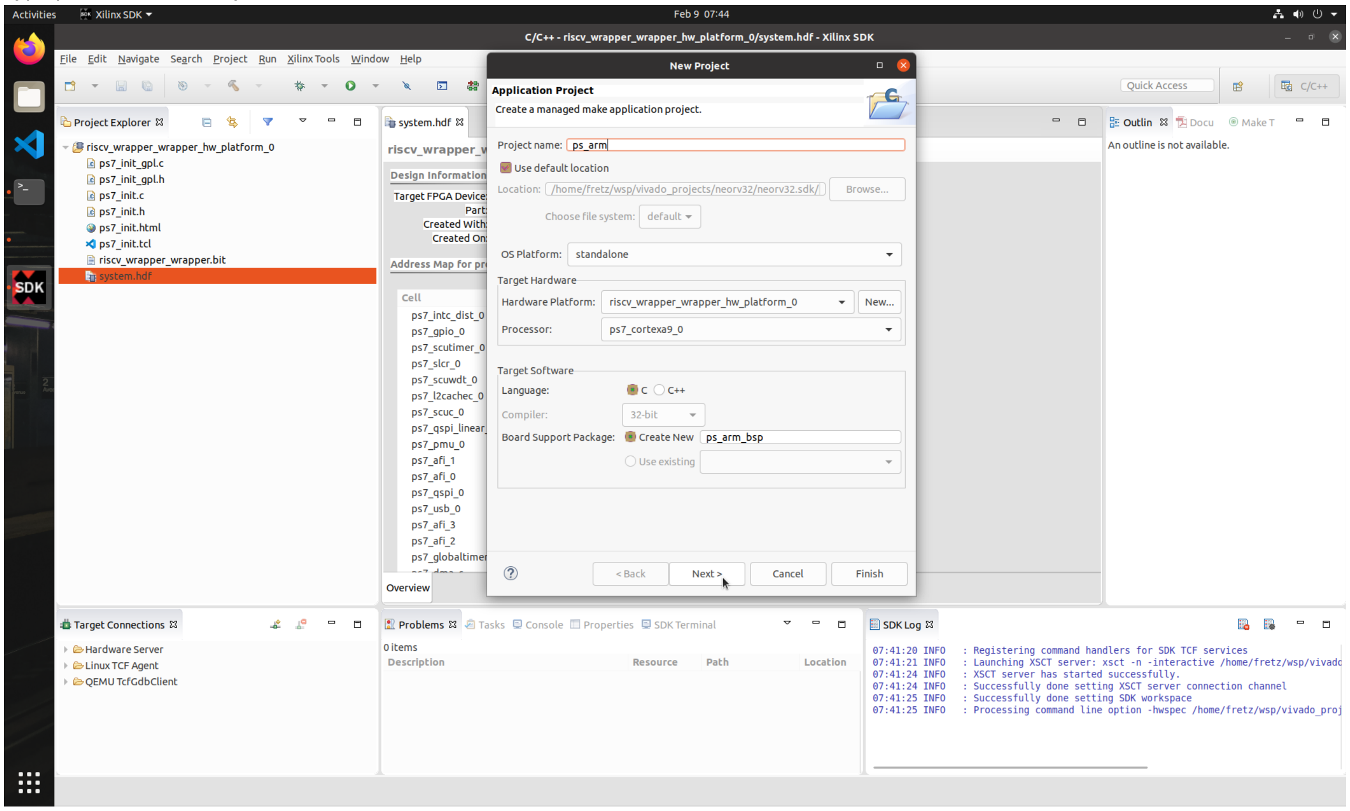
Address Map for processor ps7_cortexa9_[0-1]

Cell	Base Addr	High Addr	Slave I/f	Mem/Reg
ps7_intc_dist_0	0xf8f01000	0xf8f01fff		REGISTER
ps7_gpio_0	0xe000a000	0xe000afff		REGISTER
ps7_scutimer_0	0xf8f00600	0xf8f0061f		REGISTER
ps7_slcr_0	0xf8000000	0xf8000fff		REGISTER
ps7_scuwdt_0	0xf8f00620	0xf8f006ff		REGISTER
ps7_l2cachec_0	0xf8f02000	0xf8f02fff		REGISTER
ps7_scuc_0	0xf8f00000	0xf8f000fc		REGISTER
ps7_qspi_linear_0	0xfc000000	0xfcffffff		MEMORY
ps7_pmu_0	0xf8893000	0xf8893fff		REGISTER
ps7_afi_1	0xf8009000	0xf8009fff		REGISTER
ps7_afi_0	0xf8008000	0xf8008fff		REGISTER
ps7_qspi_0	0xe000d000	0xe000dfff		REGISTER
ps7_usb_0	0xe0002000	0xe0002fff		REGISTER
ps7_afi_3	0xf800b000	0xf800bfff		REGISTER
ps7_afi_2	0xf800a000	0xf800afff		REGISTER
ps7_globaltimer_0	0xf8f00200	0xf8f002ff		REGISTER

SDK Log

```
07:41:20 INFO   : Registering command handlers for SDK TCF services
07:41:21 INFO   : Launching XSCT server: xsct -n -interactive /home/fretz/wsp/vivado
07:41:24 INFO   : XSCT server has started successfully.
07:41:24 INFO   : Successfully done setting XSCT server connection channel
07:41:25 INFO   : Successfully done setting SDK workspace
07:41:25 INFO   : Processing command line option -hwspec /home/fretz/wsp/vivado_proj
```

- Type `ps_arm` as the Project name and click on the next button



New Project

Application Project

Create a managed make application project.

Project name:	ps_arm
Use default location	✓
Location:	/home/fretz/wsp/vivado_projects/neorv32/neorv32.sdk/
Choose file system:	default
OS Platform:	standalone

Target Hardware

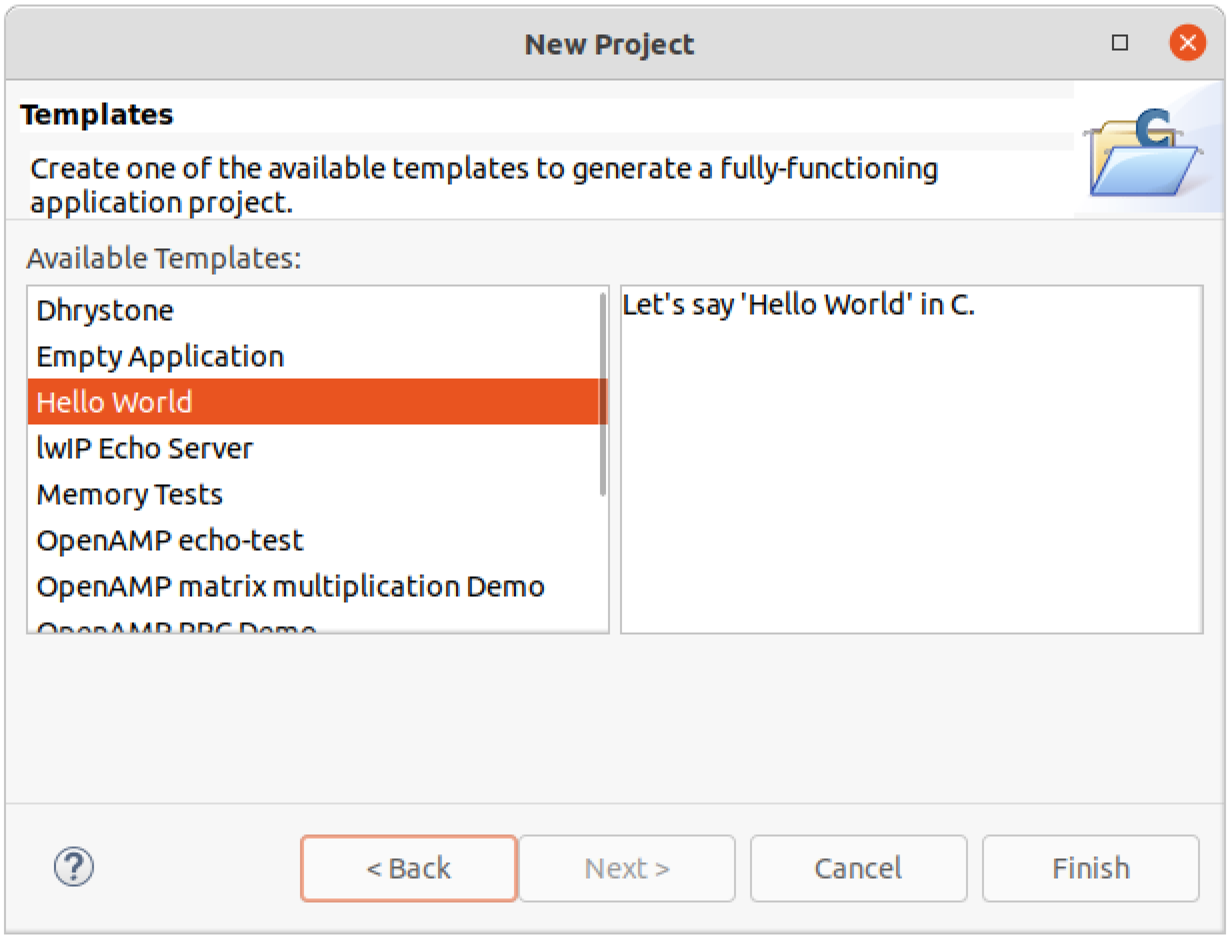
Hardware Platform:	riscv_wrapper_wrapper_hw_platform_0
Processor:	ps7_cortexa9_0

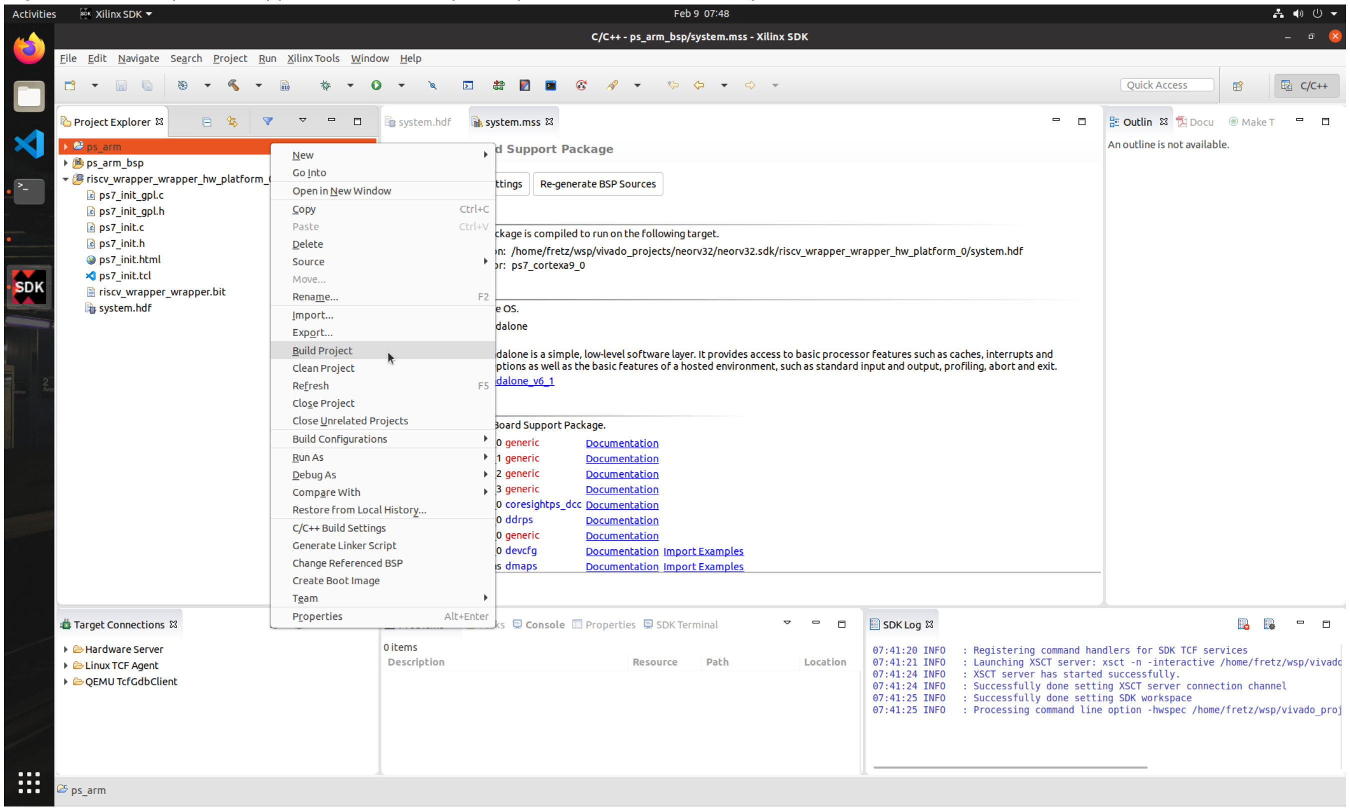
Target Software

Language:	[● C] C++
Compiler:	32-bit
Board Support Package:	[● Create New] ps_arm_bsp
	Use existing

```
07:41:20 INFO   : Registering command handlers for SDK TCF services
07:41:21 INFO   : Launching XSCT server: xsct -n -interactive /home/fretz/wsp/vivado
07:41:24 INFO   : XSCT server has started successfully.
07:41:24 INFO   : Successfully done setting XSCT server connection channel
07:41:25 INFO   : Successfully done setting SDK workspace
07:41:25 INFO   : Processing command line option -hwspec /home/fretz/wsp/vivado_proj
```

- Choose the simple Hello world example from the available code templates and click the Finish button



- Right-click on the `ps_arm` application in the Project Explorer and click Build Project
- 

d Support Package

ckage is compiled to run on the following target.
n: /home/fretz/wsp/vivado_projects/neorv32/neorv32.sdk/riscv_wrapper_wrapper_hw_platform_0/system.hdf
or: ps7_cortexa9_0

e OS.
dalone

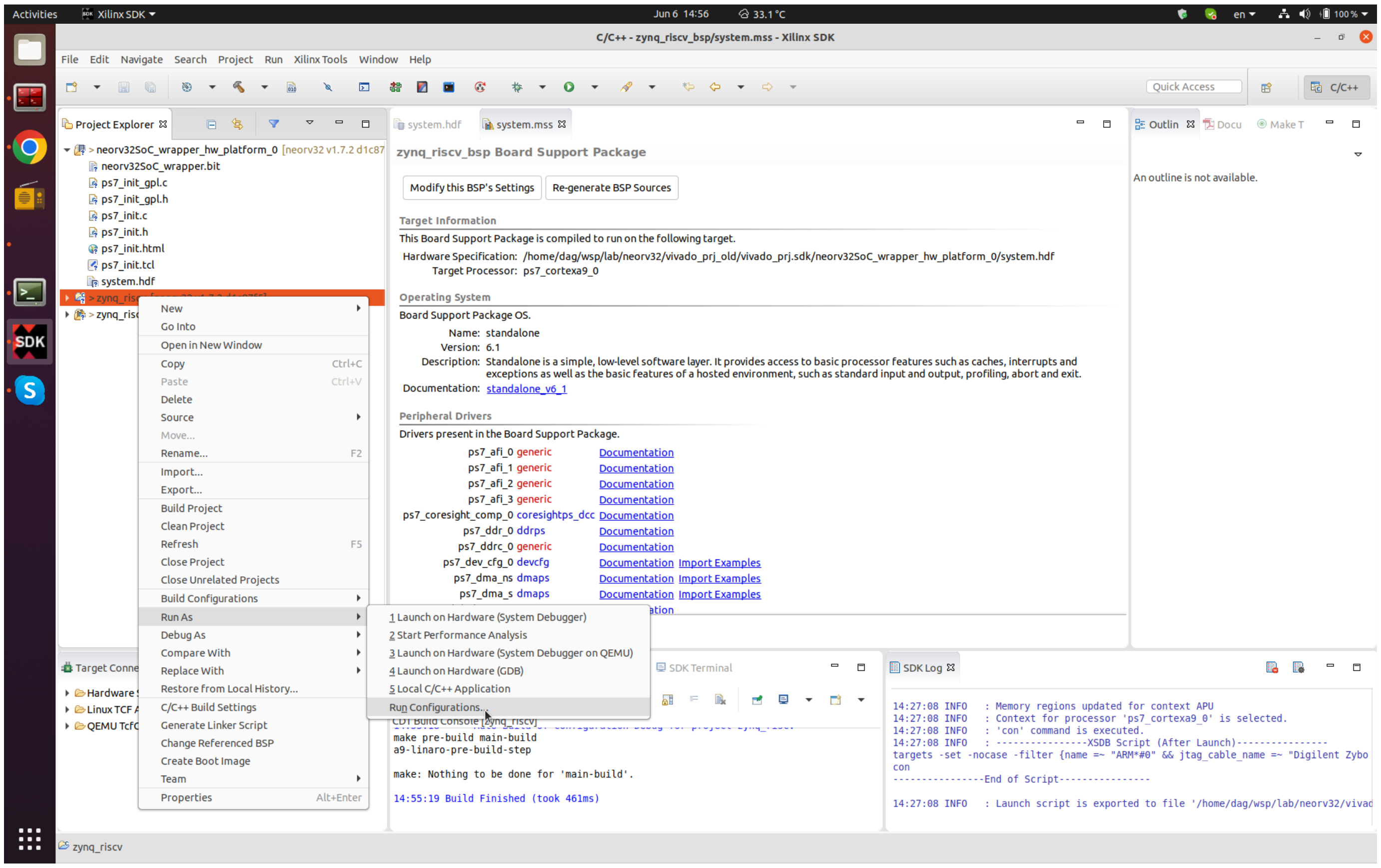
dalone is a simple, low-level software layer. It provides access to basic processor features such as caches, interrupts and
ptions as well as the basic features of a hosted environment, such as standard input and output, profiling, abort and exit.
dalone_v6_1

Board Support Package.

0 generic	Documentation
1 generic	Documentation
2 generic	Documentation
3 generic	Documentation
0 coresightps_dcc	Documentation
0 ddrps	Documentation
0 generic	Documentation
0 devcfg	Documentation Import Examples
s dmaps	Documentation Import Examples

```
07:41:20 INFO   : Registering command handlers for SDK TCF services
07:41:21 INFO   : Launching XSCT server: xsct -n -interactive /home/fretz/wsp/vivado
07:41:24 INFO   : XSCT server has started successfully.
07:41:24 INFO   : Successfully done setting XSCT server connection channel
07:41:25 INFO   : Successfully done setting SDK workspace
07:41:25 INFO   : Processing command line option -hwspec /home/fretz/wsp/vivado_proj
```

- Right-click on the `ps_arm` application in Project Explorer and click Run As Run Configuration



zynq_riscv_bsp Board Support Package

Target Information
This Board Support Package is compiled to run on the following target.
Hardware Specification: /home/dag/wsp/lab/neorv32/vivado_prj_old/vivado_prj.sdk/neorv32SoC_wrapper_hw_platform_0/system.hdf
Target Processor: ps7_cortexa9_0

Operating System
Board Support Package OS.
Name: standalone
Version: 6.1
Description: Standalone is a simple, low-level software layer. It provides access to basic processor features such as caches, interrupts and exceptions as well as the basic features of a hosted environment, such as standard input and output, profiling, abort and exit.
Documentation: standalone_v6_1

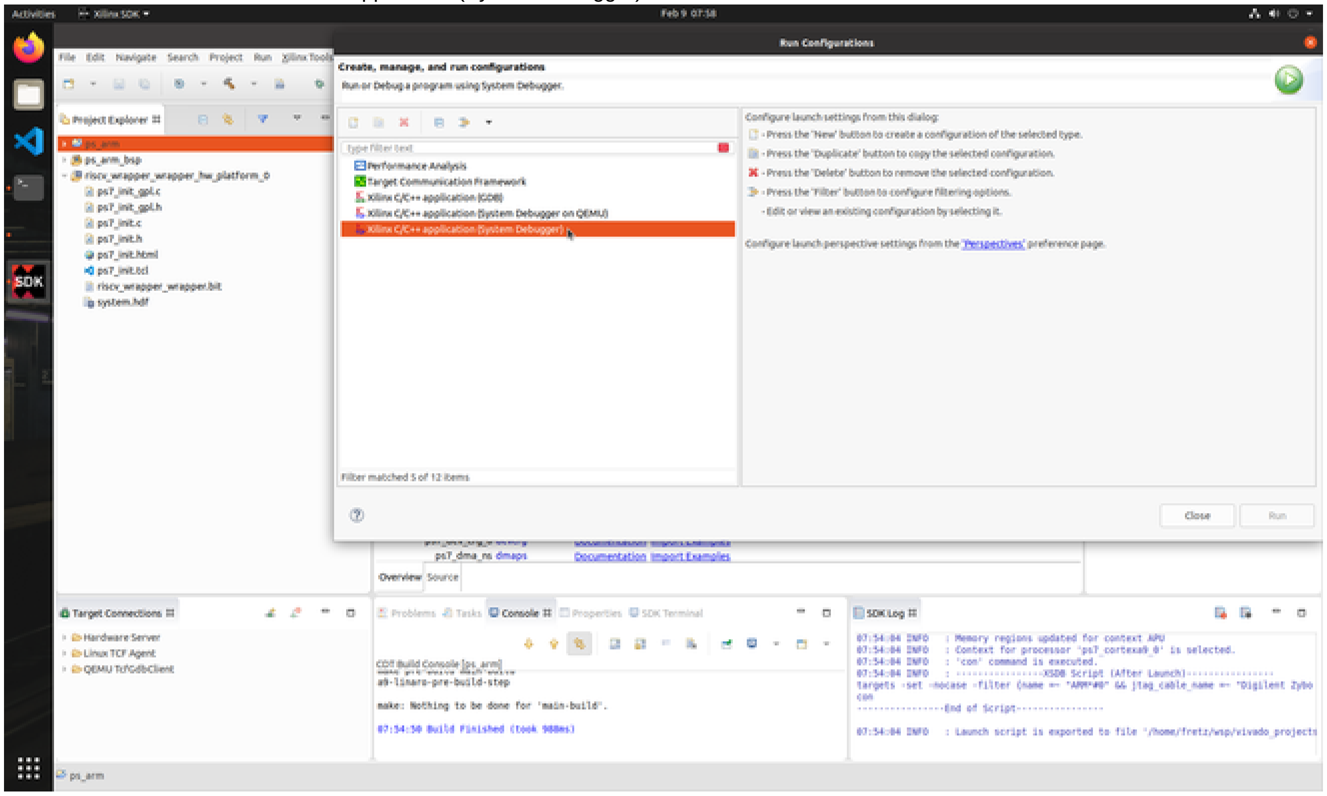
Peripheral Drivers
Drivers present in the Board Support Package.

ps7_afi_0	generic	Documentation
ps7_afi_1	generic	Documentation
ps7_afi_2	generic	Documentation
ps7_afi_3	generic	Documentation
ps7_coresight_comp_0	coresightps_dcc	Documentation
ps7_ddr_0	ddrps	Documentation
ps7_ddrc_0	generic	Documentation
ps7_dev_cfg_0	devcfg	Documentation Import Examples
ps7_dma_ns	dmaps	Documentation Import Examples
ps7_dma_s	dmaps	Documentation Import Examples

```
CDT Build Console [zynq_riscv]
make pre-build main-build
a9-linaro-pre-build-step

make: Nothing to be done for 'main-build'.

14:55:19 Build Finished (took 461ms)
```

```
14:27:08 INFO   : Memory regions updated for context APU
14:27:08 INFO   : Context for processor 'ps7_cortexa9_0' is selected.
14:27:08 INFO   : 'con' command is executed.
14:27:08 INFO   : ---------------XSDB Script (After Launch)---------------
targets -set -nocase -filter {name =~ "ARM*#0" && jtag_cable_name =~ "Digilent Zybo
con
---------------End of Script---------------

14:27:08 INFO   : Launch script is exported to file '/home/dag/wsp/lab/neorv32/vivad
```

- Double-click on the TCF Xilinx C/C++ application (System Debugger)


Run Configurations
Create, manage, and run configurations
Run or Debug a program using System Debugger.
type filter text
Performance Analysis
Target Communication Framework
Xilinx C/C++ application (GDB)
Xilinx C/C++ application (System Debugger on QEMU)
Xilinx C/C++ application (System Debugger)
Filter matched 5 of 12 items
Close
Run
Project Explorer
ps_arm
ps_arm_bsp
riscv_wrapper_wrapper_hw_platform_0
ps7_init_gpl.c
ps7_init_gpl.h
ps7_init.c
ps7_init.h
ps7_init.html
ps7_init.tcl
riscv_wrapper_wrapper.bit
system.hdf
Target Connections
Hardware Server
Linux TCF Agent
QEMU TcfGdbClient
Overview Source
Problems Tasks Console Properties SDK Terminal
SDK Log

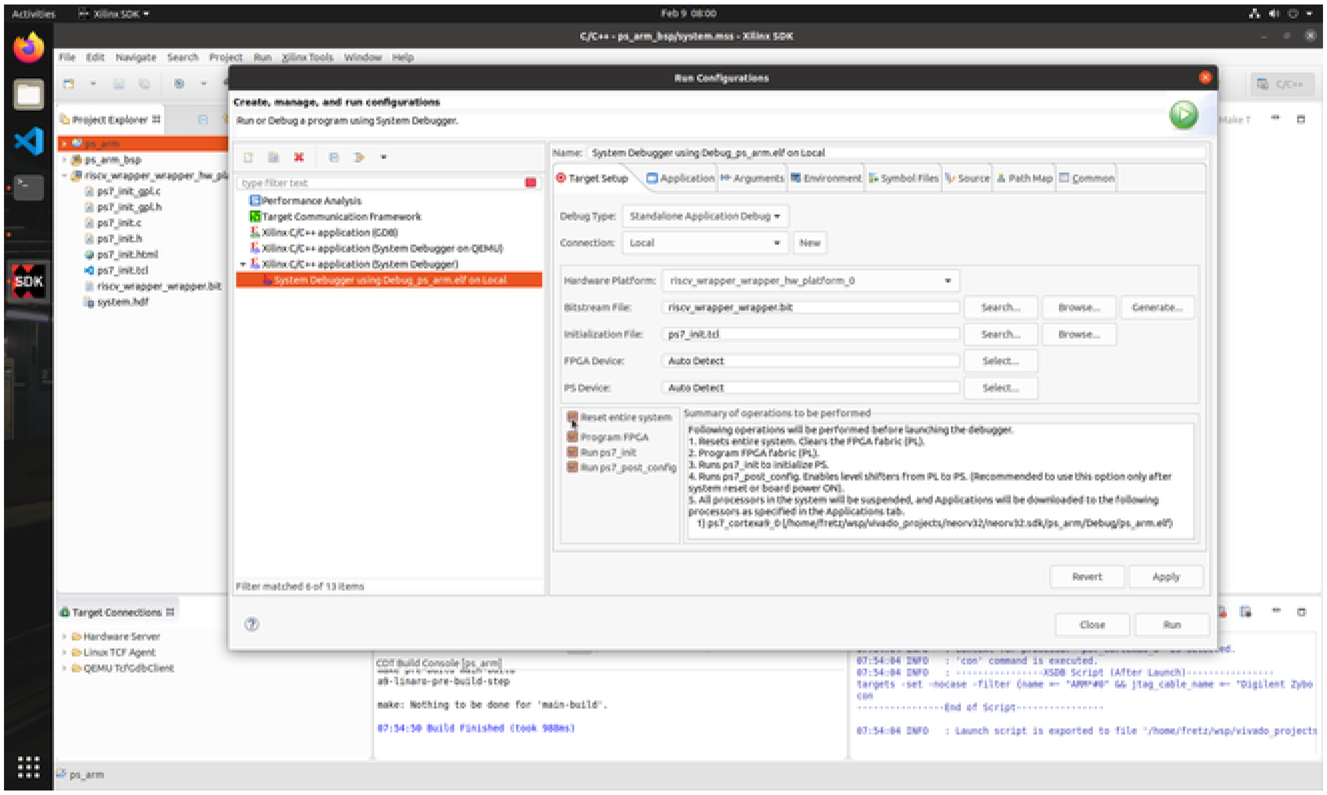
Configure launch settings from this dialog:
- Press the 'New' button to create a configuration of the selected type.
- Press the 'Duplicate' button to copy the selected configuration.
- Press the 'Delete' button to remove the selected configuration.
- Press the 'Filter' button to configure filtering options.
- Edit or view an existing configuration by selecting it.

Configure launch perspective settings from the 'Perspectives' preference page.

```
CDT Build Console [ps_arm]
a9-linaro-pre-build-step

make: Nothing to be done for 'main-build'.

07:54:50 Build Finished (took 988ms)
```

```
07:54:04 INFO   : Memory regions updated for context APU
07:54:04 INFO   : Context for processor 'ps7_cortexa9_0' is selected.
07:54:04 INFO   : 'con' command is executed.
07:54:04 INFO   : ---------------XSDB Script (After Launch)---------------
targets -set -nocase -filter {name =~ "ARM*#0" && jtag_cable_name =~ "Digilent Zybo
con
---------------End of Script---------------

07:54:04 INFO   : Launch script is exported to file '/home/fretz/wsp/vivado_projects
```

- Select the Reset entire system, click on the Apply button and then on the Run button


Run Configurations

Create, manage, and run configurations

Run or Debug a program using System Debugger.

Name: System Debugger using Debug_ps_arm.elf on Local

Debug Type: Standalone Application Debug

Connection: Local

Hardware Platform: riscv_wrapper_wrapper_hw_platform_0

Bitstream File: riscv_wrapper_wrapper.bit

Initialization File: ps7_init.tcl

FPGA Device: Auto Detect

PS Device: Auto Detect

[✓] Reset entire system
[✓] Program FPGA
[✓] Run ps7_init
[✓] Run ps7_post_config

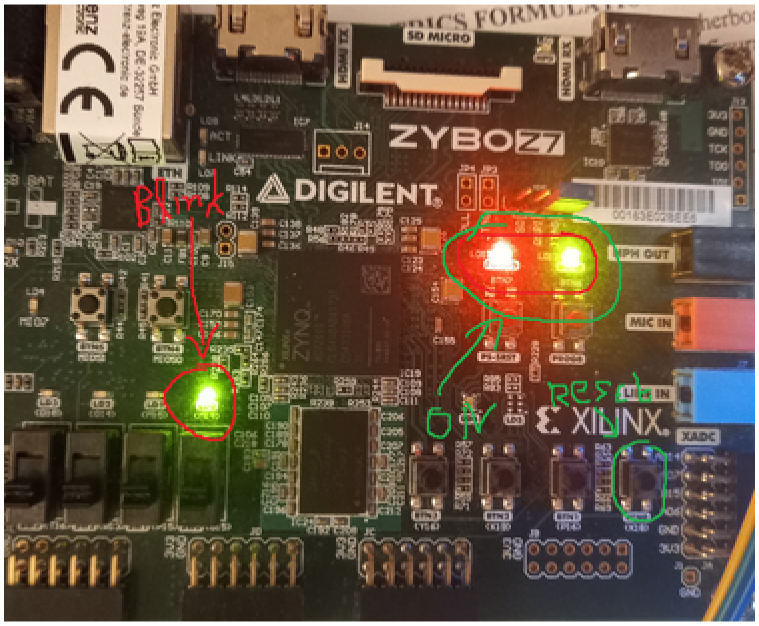
Summary of operations to be performed

Following operations will be performed before launching the debugger.
1. Resets entire system. Clears the FPGA fabric (PL).
2. Program FPGA fabric (PL).
3. Runs ps7_init to initialize PS.
4. Runs ps7_post_config. Enables level shifters from PL to PS. (Recommended to use this option only after system reset or board power ON).
5. All processors in the system will be suspended, and Applications will be downloaded to the following processors as specified in the Applications tab.
1) ps7_cortexa9_0 (/home/fretz/wsp/vivado_projects/neorv32/neorv32.sdk/ps_arm/Debug/ps_arm.elf)

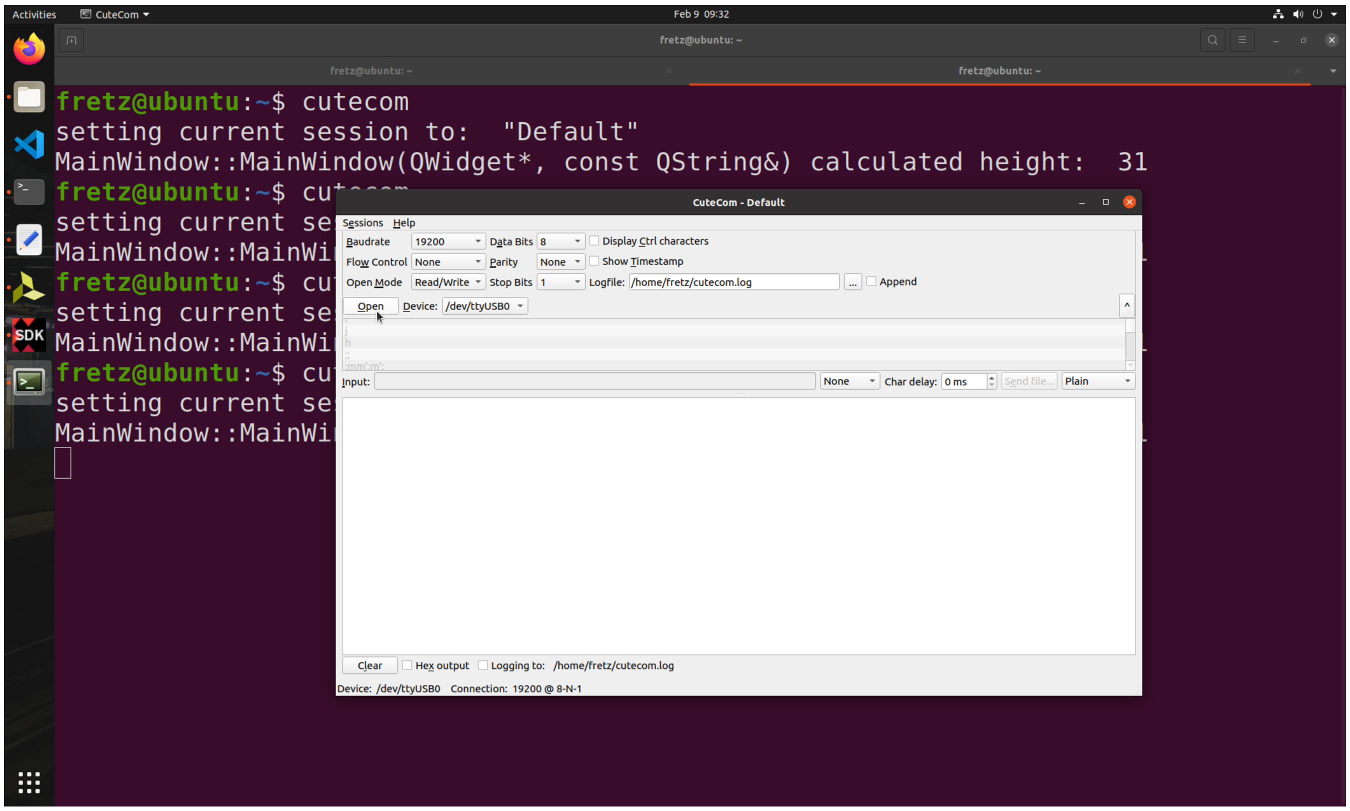
```
a9-linaro-pre-build-step

make: Nothing to be done for 'main-build'.

07:54:50 Build Finished (took 988ms)
```

```
07:54:04 INFO   : 'con' command is executed.
07:54:04 INFO   : ----------------XSDB Script (After Launch)----------------
targets -set -nocase -filter {name =~ "ARM*#0" && jtag_cable_name =~ "Digilent Zybo
con
----------------End of Script----------------

07:54:04 INFO   : Launch script is exported to file '/home/fretz/wsp/vivado_projects
```

- Once you program the FPGA you should see that the LD0 blinks (left side of the photo) after you press the reset button (right side of the photo). Also, the PGOOD and DONE leds should be ON.



- Open a terminal and press `cutecom`
- Click on settings and configure as follows and then click on open

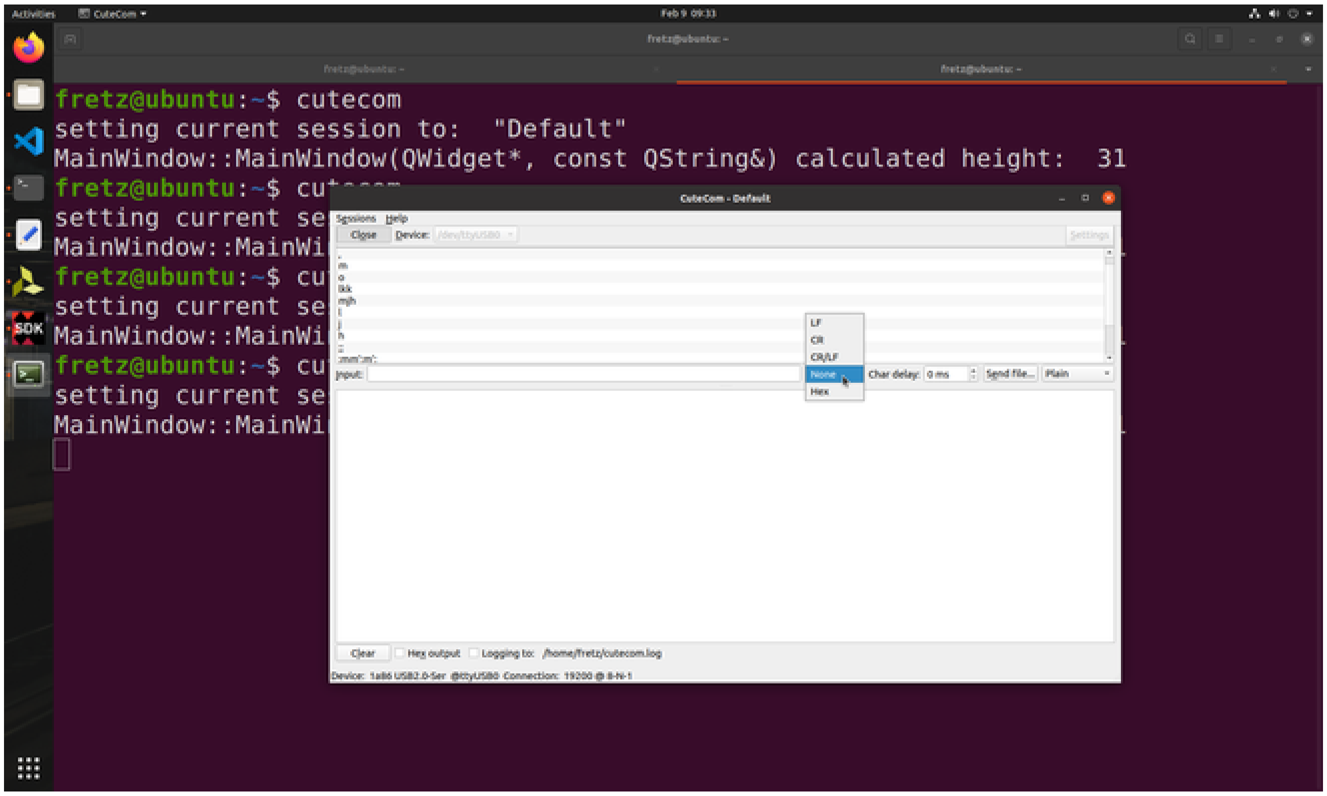


```
fretz@ubuntu:~$ cutecom
setting current session to:  "Default"
MainWindow::MainWindow(QWidget*, const QString&) calculated height:  31
fretz@ubuntu:~$ cu
setting current se
MainWindow::MainWi
fretz@ubuntu:~$ cu
setting current se
MainWindow::MainWi
fretz@ubuntu:~$ cu
setting current se
MainWindow::MainWi
```

CuteCom - Default

Baudrate: 19200 — Data Bits: 8 — Display Ctrl characters
Flow Control: None — Parity: None — Show Timestamp
Open Mode: Read/Write — Stop Bits: 1 — Logfile: /home/fretz/cutecom.log — Append
Open — Device: /dev/ttyUSB0
Input: — None — Char delay: 0 ms — Send file... — Plain
Clear — Hex output — Logging to: /home/fretz/cutecom.log
Device: /dev/ttyUSB0 Connection: 19200 @ 8-N-1

- Select None



```
fretz@ubuntu:~$ cutecom
setting current session to:  "Default"
MainWindow::MainWindow(QWidget*, const QString&) calculated height:  31
fretz@ubuntu:~$ cu
setting current se
MainWindow::MainWi
fretz@ubuntu:~$ cu
setting current se
MainWindow::MainWi
fretz@ubuntu:~$ cu
setting current se
MainWindow::MainWi
```

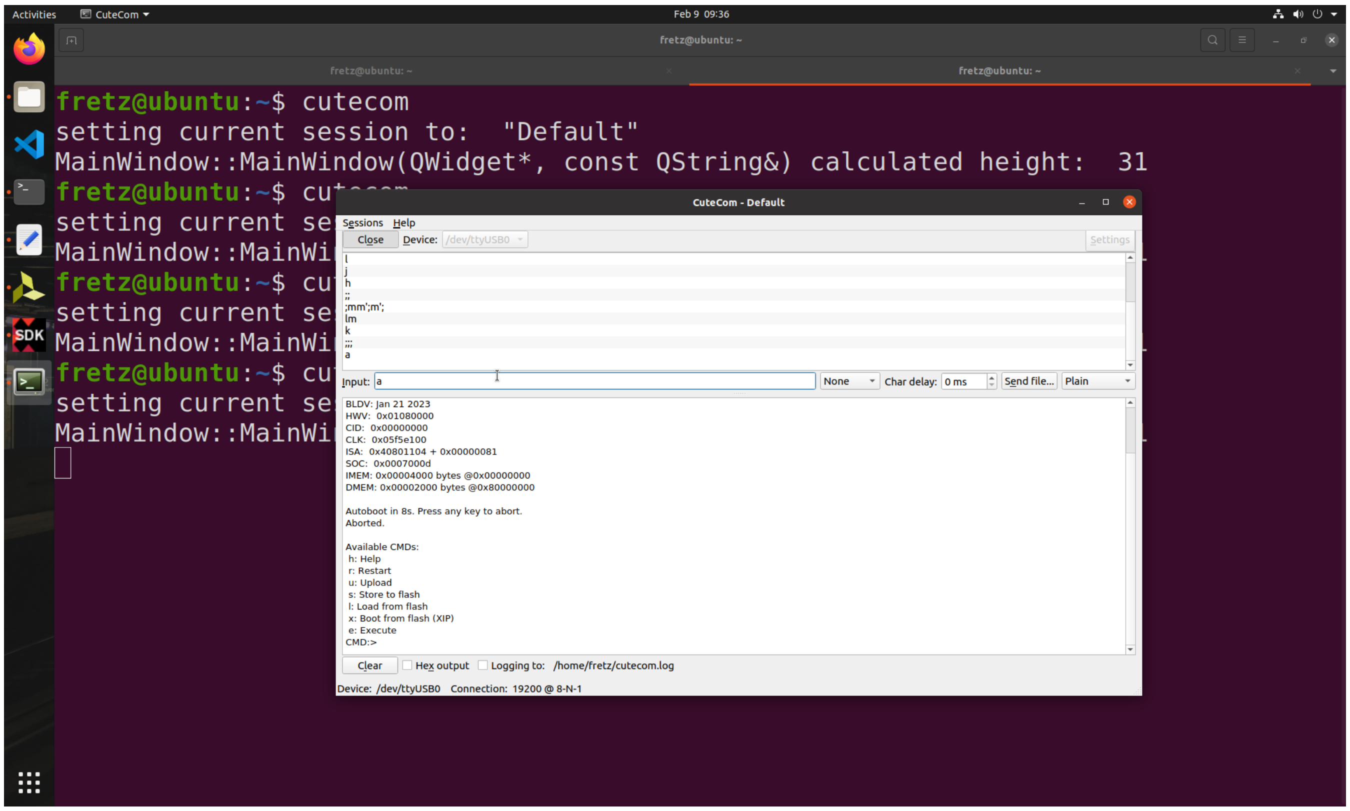
CuteCom - Default

Close — Device: /dev/ttyUSB0 — Settings

```
m
o
lkk
mjh
l
j
h
:mm':m':
```

Input: — Char delay: 0 ms — Send file... — Plain
Clear — Hex output — Logging to: /home/fretz/cutecom.log
Device: 1a86 USB2.0-Ser @ttyUSB0 Connection: 19200 @ 8-N-1

- In the input add the character a, press the reset button of NEORV32-V on the board and then press enter on cutecom
-



```
fretz@ubuntu:~$ cutecom
setting current session to:  "Default"
MainWindow::MainWindow(QWidget*, const QString&) calculated height:  31
fretz@ubuntu:~$ cutecom
setting current se
MainWindow::MainWi
fretz@ubuntu:~$ cu
setting current se
MainWindow::MainWi
fretz@ubuntu:~$ cu
setting current se
MainWindow::MainWi
```

Device: /dev/ttyUSB0

```
l
j
h
;;
;mm';m';
lm
k
;;;
a
```

Input: a | None | Char delay: 0 ms | Plain

```
BLDV: Jan 21 2023
HWV:  0x01080000
CID:  0x00000000
CLK:  0x05f5e100
ISA:  0x40801104 + 0x00000081
SOC:  0x0007000d
IMEM: 0x00004000 bytes @0x00000000
DMEM: 0x00002000 bytes @0x80000000

Autoboot in 8s. Press any key to abort.
Aborted.

Available CMDs:
 h: Help
 r: Restart
 u: Upload
 s: Store to flash
 l: Load from flash
 x: Boot from flash (XIP)
 e: Execute
CMD:>
```

Hex output | Logging to: /home/fretz/cutecom.log

Device: /dev/ttyUSB0   Connection: 19200 @ 8-N-1

Setup RISC-V compiler

Skip these steps if you have the Fretz virtual machine.

- Open the Fretz VM and install `cutecom`, and the RISC-V compile flow
- In a terminal type, the following

```
$ sudo apt install cutecom -y
$ cd ~/wsp/Downloads/
$ wget https://github.com/stnolting/riscv-gcc-prebuilt/releases/download
/rv32i-2.0.0/riscv32-unknown-elf.gcc-10.2.0.rv32i.ilp32.newlib.tar.gz
```

Create a folder where you want to install the toolchain, for example `/opt/riscv` (you will need `sudo` rights to create this folder and copy data to it).

```
$ sudo mkdir /opt/riscv
```

Navigate to the download folder. Decompress your toolchain (replace `TOOLCHAIN` with your toolchain archive of choice). Again, you might have to use `sudo` if your target directory is protected.

```
$ sudo tar xzfv riscv32-unknown-elf.gcc-10.2.0.rv32i.ilp32.newlib.tar.
gz -C /opt/riscv/
```

Now add the toolchain's `bin` folder to your system's `PATH` environment variable (or add this line to your `.bashrc` if applicable):

```
$ export PATH=$PATH:/opt/riscv/bin
```

Test the toolchain:

```
$ riscv32-unknown-elf-gcc -v
```

Continue from here: Compile your first hello world example!!!!

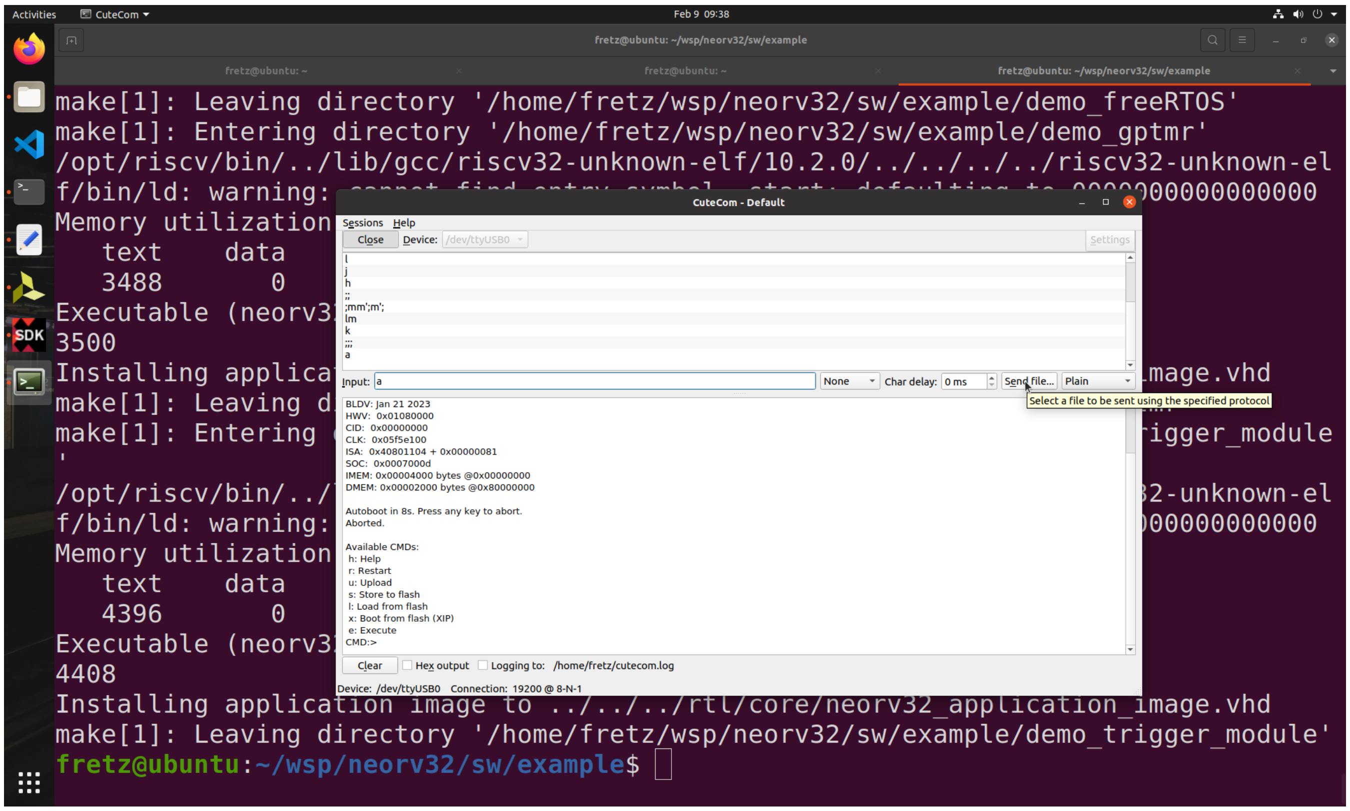
- Let's download some application examples. Open a terminal and type

```
cd ~/wsp/neorv32/sw/examples
make clean_all
make all
```

- On cutecome enter the character u and press enter

```
CMD:> u
Awaiting neorv32_exe.bin...
```

- On cutecome click the send file button



```
make[1]: Leaving directory '/home/fretz/wsp/neorv32/sw/example/demo_freeRTOS'
make[1]: Entering directory '/home/fretz/wsp/neorv32/sw/example/demo_gptmr'
/opt/riscv/bin/../lib/gcc/riscv32-unknown-elf/10.2.0/../../../../riscv32-unknown-el
f/bin/ld: warning:
Memory utilization
   text     data
   3488        0
Executable (neorv3
3500
Installing applica                                                          image.vhd
make[1]: Leaving d
make[1]: Entering                                                         rigger_module
'
/opt/riscv/bin/../                                                        2-unknown-el
f/bin/ld: warning:                                                        000000000000
Memory utilization
   text     data
   4396        0
Executable (neorv3
4408
Installing application image to ../../../rtl/core/neorv32_application_image.vhd
make[1]: Leaving directory '/home/fretz/wsp/neorv32/sw/example/demo_trigger_module'
fretz@ubuntu:~/wsp/neorv32/sw/example$
```

```
l
j
h
;;
;mm';m';
lm
k
;;;
a
```

Input: a

```
BLDV: Jan 21 2023
HWV:  0x01080000
CID:  0x00000000
CLK:  0x05f5e100
ISA:  0x40801104 + 0x00000081
SOC:  0x0007000d
IMEM: 0x00004000 bytes @0x00000000
DMEM: 0x00002000 bytes @0x80000000

Autoboot in 8s. Press any key to abort.
Aborted.

Available CMDs:
 h: Help
 r: Restart
 u: Upload
 s: Store to flash
 l: Load from flash
 x: Boot from flash (XIP)
 e: Execute
CMD:>
```

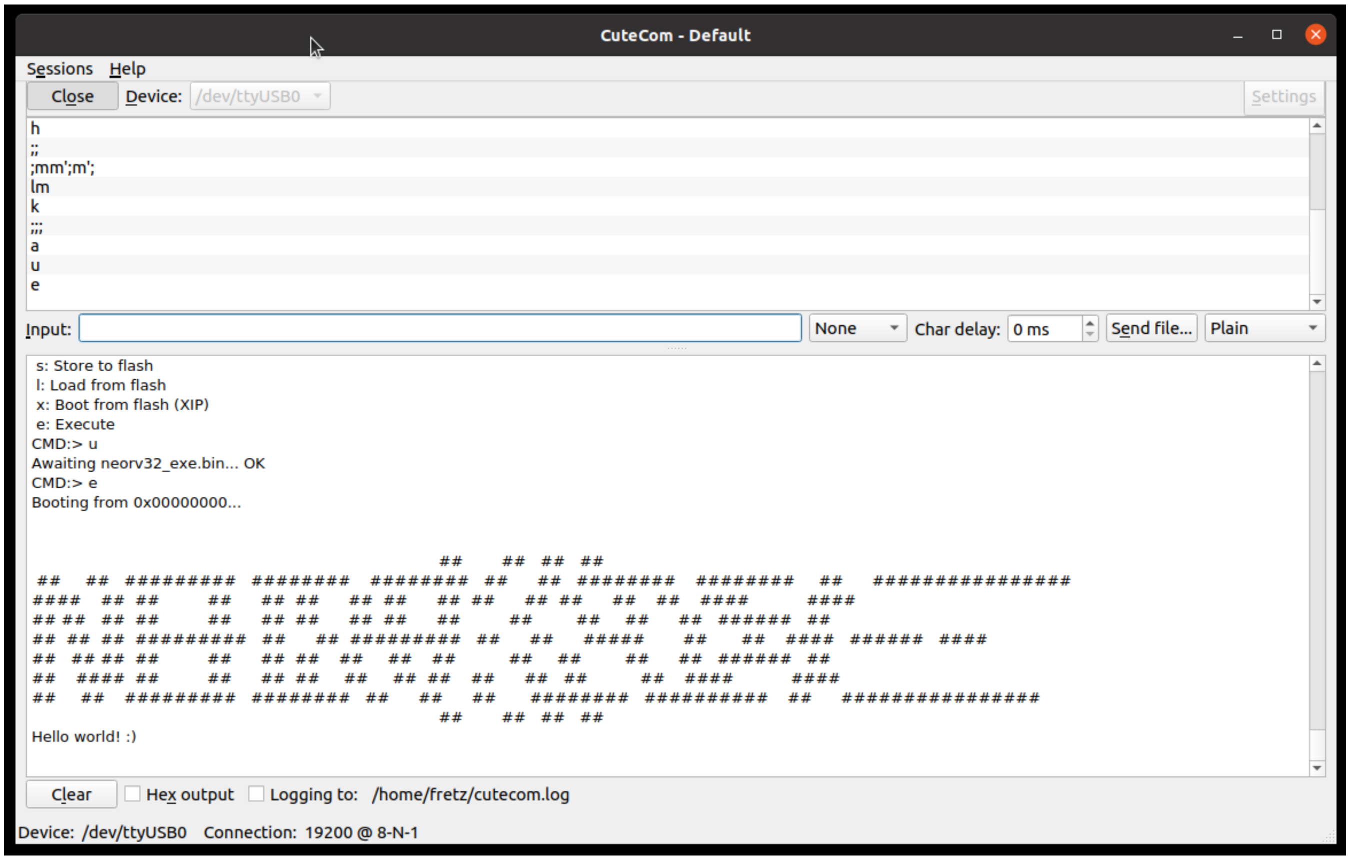
Logging to: /home/fretz/cutecom.log

Device: /dev/ttyUSB0   Connection: 19200 @ 8-N-1

- If everything goes fine, OK will appear in your terminal:

```
CMD:> u
Awaiting neorv32_exe.bin... OK
```

- The executable is now in the instruction memory of the processor. To execute the program right now, run the "Execute" command by typing e in cutecome and press the Enter on your keyboard:



```
h
;;
;mm';m';
lm
k
;;;
a
u
e
```

```
 s: Store to flash
 l: Load from flash
 x: Boot from flash (XIP)
 e: Execute
CMD:> u
Awaiting neorv32_exe.bin... OK
CMD:> e
Booting from 0x00000000...


                                                                                ##        ##   ##   ##
 ##     ##   #########   ########    ########   ##      ##   ########    ########     ##   ################
####    ##  ##          ##      ##  ##      ##  ##      ##  ##      ##  ##      ##    ##  ####        ####
## ##   ##  ##          ##      ##  ##      ##  ##      ##          ##         ##     ##  ##  ######  ##
##  ##  ##  #########   ##      ##  #########   ##      ##      #####        ##       ##  ####  ######  ####
##   ## ##  ##          ##      ##  ##    ##     ##    ##           ##     ##         ##  ##  ######  ##
##    ####  ##          ##      ##  ##     ##     ##  ##    ##      ##   ##           ##  ####        ####
##     ##   #########    ########   ##      ##      ##       ########   ##########    ##   ################
                                                                                ##        ##   ##   ##
Hello world! :)
```

Device: /dev/ttyUSB0   Connection: 19200 @ 8-N-1