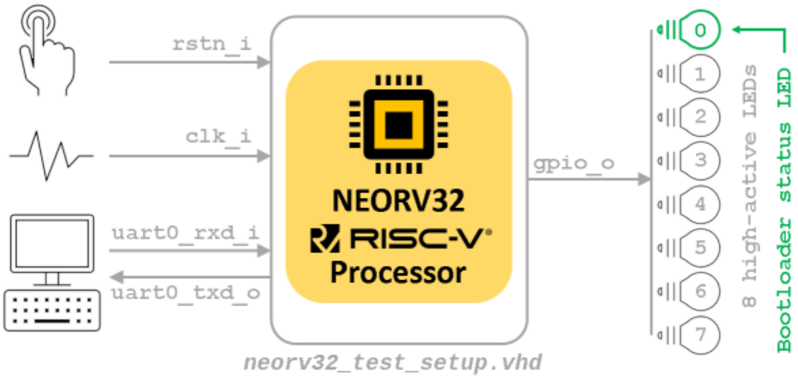
NEORV32 RISC-V on Digilent Basys3

This tutorial will guide you through implementing the RISC-V “neorv32” processor on the Digilent Basys3 FPGA board.



You can find additional information for the NEORV-32 microarchitecture in the following links

- [Datasheet] The NEORV32 RISC-V Processor
- [User Guide] The NEORV32 RISC-V Processor
- https://github.com/stnolting/neorv32/tree/v1.11.0 Can't find link
- On eClass - Τμήμα Πληροφορικής | Embedded Systems | Έγγραφα

Hardware implementation

Follow step 1 only if you are not using the provided VM

1. Download and unzip in a folder called neorv32

```
https://github.com/stnolting/neorv32/archive/refs/tags/v1.11.0.zip
```

Beautiful, we now have the source code for NEORV-32. Let’s open Vivado to implement the processor

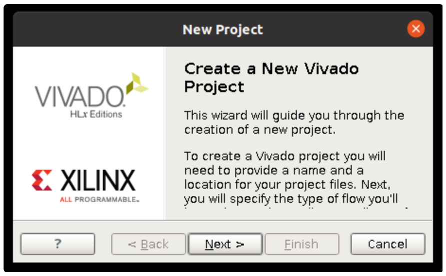
2. Open Vivado

For Linux

```
cd
cd wsp
mkdir -p vivado_projects
cd vivado_projects
source /opt/Xilinx/Vivado/2016.4/settings64.sh
vivado &
```

In MS Windows and the provided VM you open vivado by clinking the Vivado shortcut

3. Create a new project. Click from the Vivado menu File → New project and click on the next button

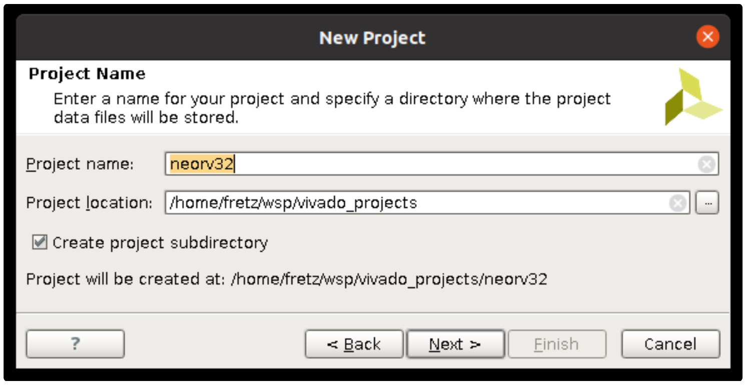


Create a New Vivado Project

This wizard will guide you through the creation of a new project.

To create a Vivado project you will need to provide a name and a location for your project files. Next, you will specify the type of flow you'll

- Type neorv32 as the project name



Project Name

Enter a name for your project and specify a directory where the project data files will be stored.

Project name: neorv32

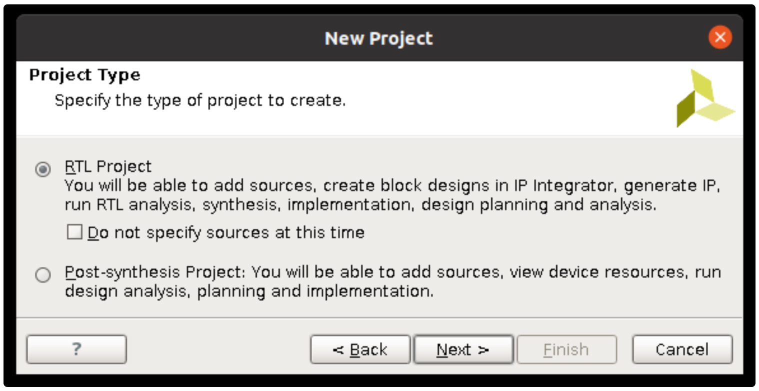
Project location: /home/fretz/wsp/vivado_projects

☑ Create project subdirectory

Project will be created at: /home/fretz/wsp/vivado_projects/neorv32

- Choose the RTL project

⚠ BE CAREFUL → Unselect the do not specify sources at this time



Project Type

Specify the type of project to create.

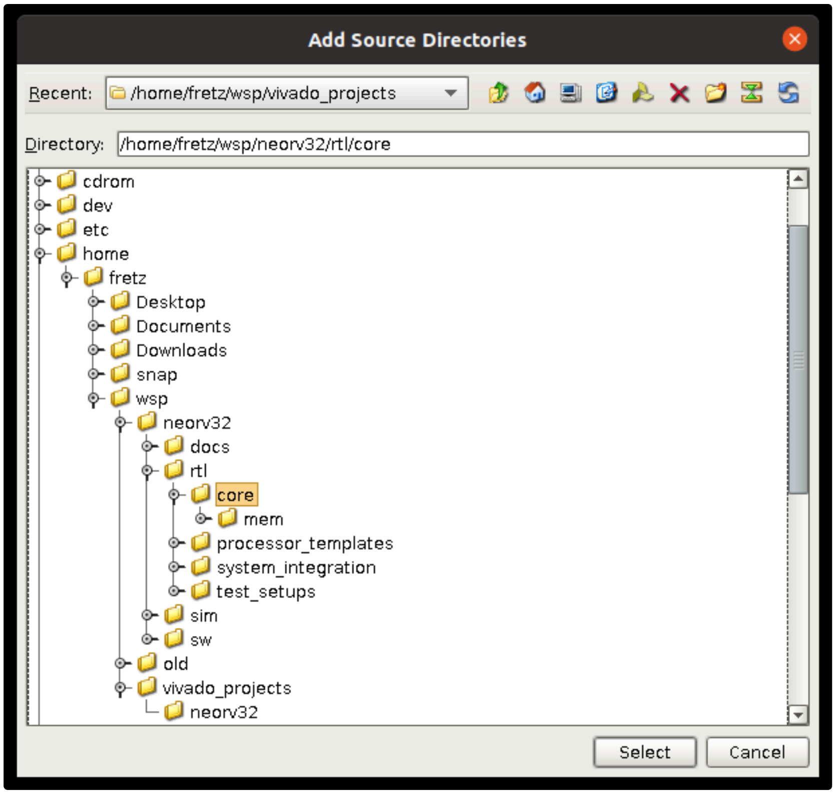
● RTL Project
You will be able to add sources, create block designs in IP Integrator, generate IP, run RTL analysis, synthesis, implementation, design planning and analysis.

□ Do not specify sources at this time

○ Post-synthesis Project: You will be able to add sources, view device resources, run design analysis, planning and implementation.

- Choose as target language **VHDL** and click on the **Add Directories** button to add the VHDL source code of the NEORV-32

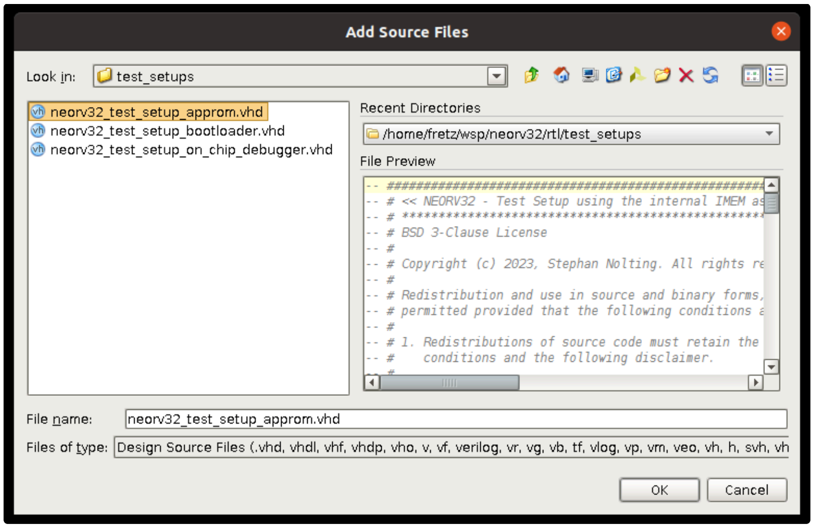
- Choose the Directory → `neorv32/rtl/core/`

- 

  Recent: /home/fretz/wsp/vivado_projects

  Directory: /home/fretz/wsp/neorv32/rtl/core

- Click on the **Add Files** button to add one more source code. Choose `neorv32/rtl/test_setups/neorv32_test_setup_bootloader.vhd` and click on the OK button

  
  Add Source Files
neorv32_test_setup_approm.vhd
neorv32_test_setup_bootloader.vhd
neorv32_test_setup_on_chip_debugger.vhd
Recent Directories
File Preview
OK
Cancel

  Look in: test_setups

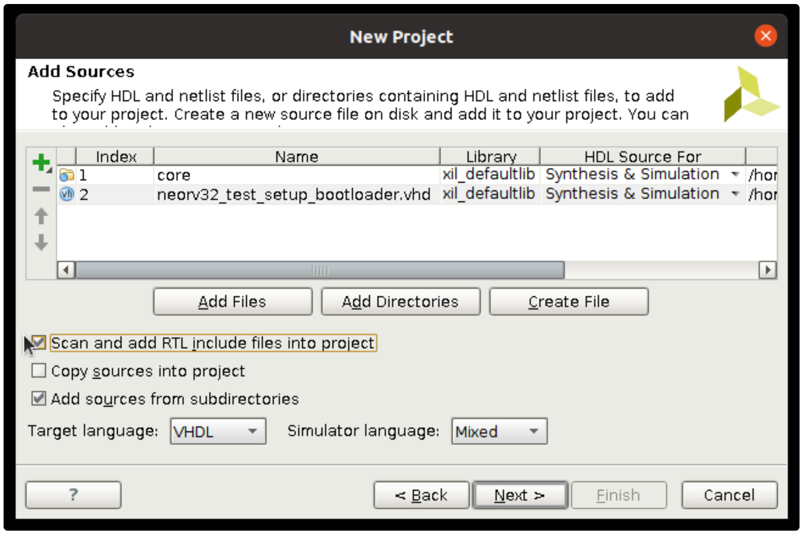
  Recent Directories: /home/fretz/wsp/neorv32/rtl/test_setups

  ```
  -- #################################################
  -- # << NEORV32 - Test Setup using the internal IMEM as
  -- # ************************************************
  -- # BSD 3-Clause License
  -- #
  -- # Copyright (c) 2023, Stephan Nolting. All rights re
  -- #
  -- # Redistribution and use in source and binary forms,
  -- # permitted provided that the following conditions a
  -- #
  -- # 1. Redistributions of source code must retain the
  -- #    conditions and the following disclaimer.
  ```

  File name: neorv32_test_setup_approm.vhd

  Files of type: Design Source Files (.vhd, vhdl, vhf, vhdp, vho, v, vf, verilog, vr, vg, vb, tf, vlog, vp, vm, veo, vh, h, svh, vh

- Tick the Scan and add RTL include files into the project, and finally click on the NEXT button



Add Sources

Specify HDL and netlist files, or directories containing HDL and netlist files, to add to your project. Create a new source file on disk and add it to your project. You can

Index	Name	Library	HDL Source For	
1	core	xil_defaultlib	Synthesis & Simulation	/hor
2	neorv32_test_setup_bootloader.vhd	xil_defaultlib	Synthesis & Simulation	/hor

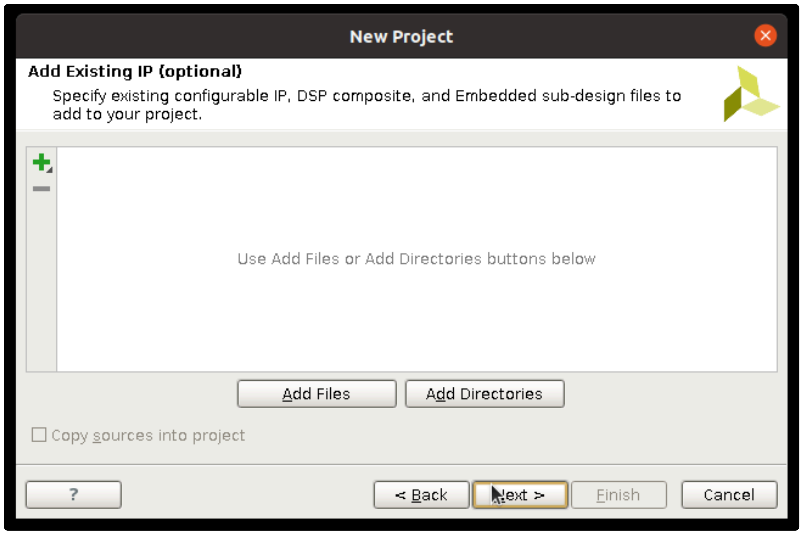
☑ Scan and add RTL include files into project

□ Copy sources into project

☑ Add sources from subdirectories

Target language: VHDL Simulator language: Mixed

- Click next on the Add Existing IP (optional)



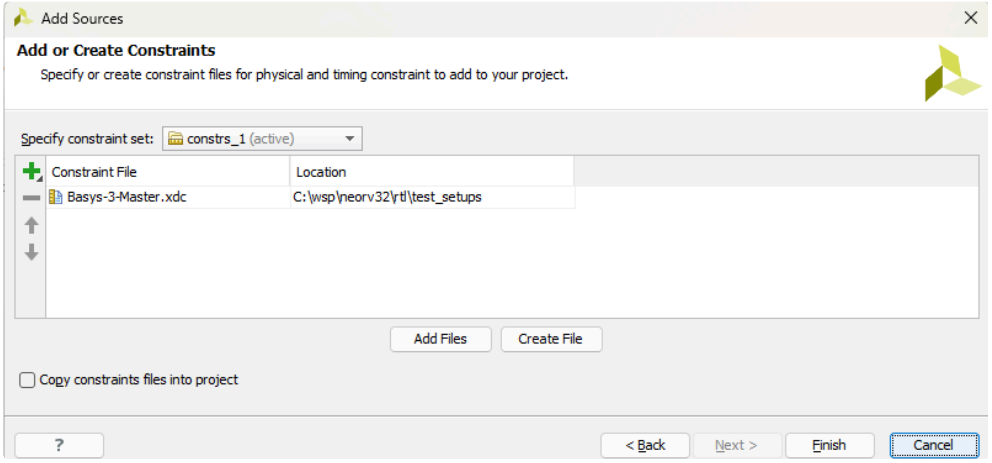
Add Existing IP (optional)

Specify existing configurable IP, DSP composite, and Embedded sub-design files to add to your project.

Use Add Files or Add Directories buttons below

□ Copy sources into project

- Download Basys XDC file from Basys-3-Master.xdc into neorv32\rtl\test_setups
- Click on the Add Files on the Add Constraints window and Press Next



Add or Create Constraints

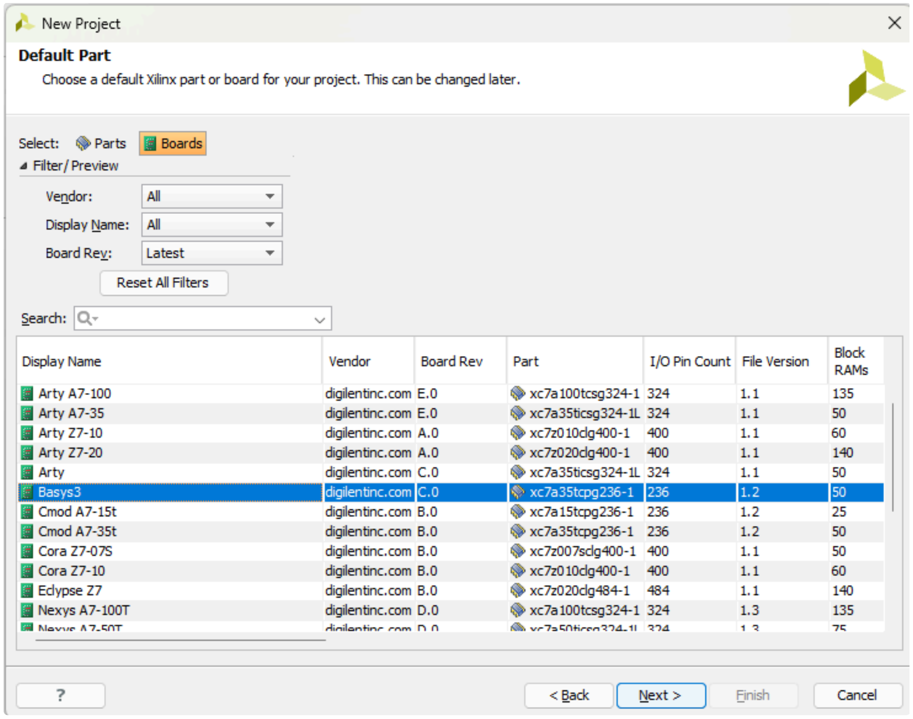
Specify or create constraint files for physical and timing constraint to add to your project.

Specify constraint set: constrs_1 (active)

Constraint File	Location
Basys-3-Master.xdc	C:\wsp\neorv32\rtl\test_setups

□ Copy constraints files into project

- Click on Boards and choose the Basys



Default Part

Choose a default Xilinx part or board for your project. This can be changed later.

Select: Parts **Boards**

Filter/ Preview

Vendor: All

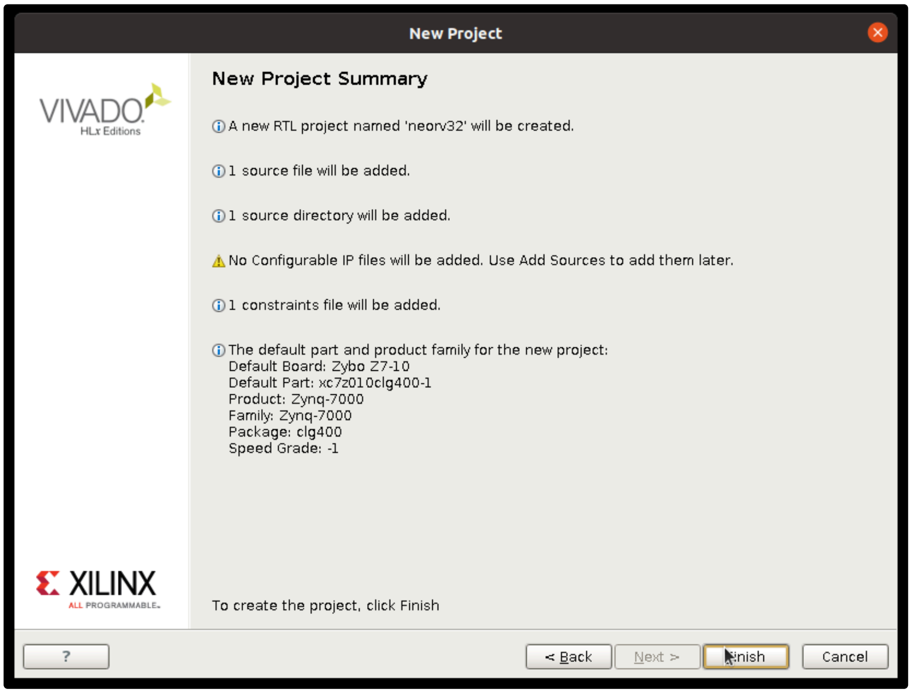
Display Name: All

Board Rev: Latest

Search:

Display Name	Vendor	Board Rev	Part	I/O Pin Count	File Version	Block RAMs
Arty A7-100	digilentinc.com	E.0	xc7a100tcsg324-1	324	1.1	135
Arty A7-35	digilentinc.com	E.0	xc7a35ticsg324-1L	324	1.1	50
Arty Z7-10	digilentinc.com	A.0	xc7z010clg400-1	400	1.1	60
Arty Z7-20	digilentinc.com	A.0	xc7z020clg400-1	400	1.1	140
Arty	digilentinc.com	C.0	xc7a35ticsg324-1L	324	1.1	50
Basys3	digilentinc.com	C.0	xc7a35tcpg236-1	236	1.2	50
Cmod A7-15t	digilentinc.com	B.0	xc7a15tcpg236-1	236	1.2	25
Cmod A7-35t	digilentinc.com	B.0	xc7a35tcpg236-1	236	1.2	50
Cora Z7-07S	digilentinc.com	B.0	xc7z007sclg400-1	400	1.1	50
Cora Z7-10	digilentinc.com	B.0	xc7z010clg400-1	400	1.1	60
Eclypse Z7	digilentinc.com	B.0	xc7z020clg484-1	484	1.1	140
Nexys A7-100T	digilentinc.com	D.0	xc7a100tcsg324-1	324	1.3	135
Nexys A7-50T	digilentinc.com	D.0	xc7a50ticsg324-1L	324	1.3	75

- Finally, click on the Finish button



New Project Summary

ⓘ A new RTL project named 'neorv32' will be created.

ⓘ 1 source file will be added.

ⓘ 1 source directory will be added.

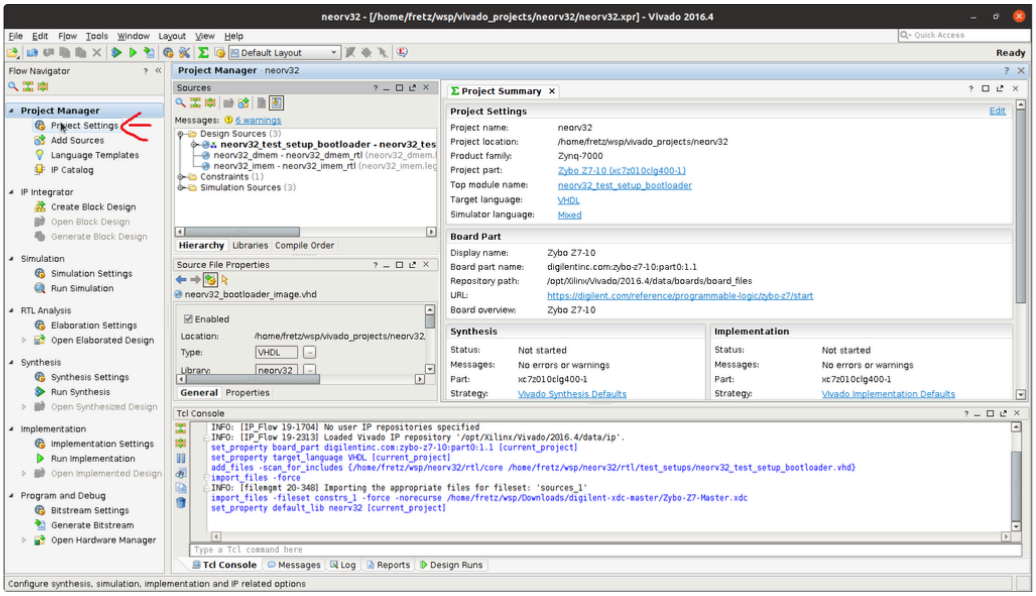
⚠ No Configurable IP files will be added. Use Add Sources to add them later.

ⓘ 1 constraints file will be added.

ⓘ The default part and product family for the new project:
Default Board: Zybo Z7-10
Default Part: xc7z010clg400-1
Product: Zynq-7000
Family: Zynq-7000
Package: clg400
Speed Grade: -1

To create the project, click Finish

- Select the Project Settings under the Project Manager



Messages: 6 warnings

- Design Sources (3)
  - neorv32_test_setup_bootloader - neorv32_tes…
    - neorv32_dmem - neorv32_dmem_rtl (neorv32_dmem.…
    - neorv32_imem - neorv32_imem_rtl (neorv32_imem.leg…
- Constraints (1)
- Simulation Sources (3)

neorv32_bootloader_image.vhd

☑ Enabled
Location: /home/fretz/wsp/vivado_projects/neorv32.
Type: VHDL
Library: neorv32

Project Settings

Project name: neorv32
Project location: /home/fretz/wsp/vivado_projects/neorv32
Product family: Zynq-7000
Project part: Zybo Z7-10 (xc7z010clg400-1)
Top module name: neorv32_test_setup_bootloader
Target language: VHDL
Simulator language: Mixed

Board Part

Display name: Zybo Z7-10
Board part name: digilentinc.com:zybo-z7-10:part0:1.1
Repository path: /opt/Xilinx/Vivado/2016.4/data/boards/board_files
URL: https://digilent.com/reference/programmable-logic/zybo-z7/start
Board overview: Zybo Z7-10

Synthesis

Status: Not started
Messages: No errors or warnings
Part: xc7z010clg400-1
Strategy: Vivado Synthesis Defaults

Implementation

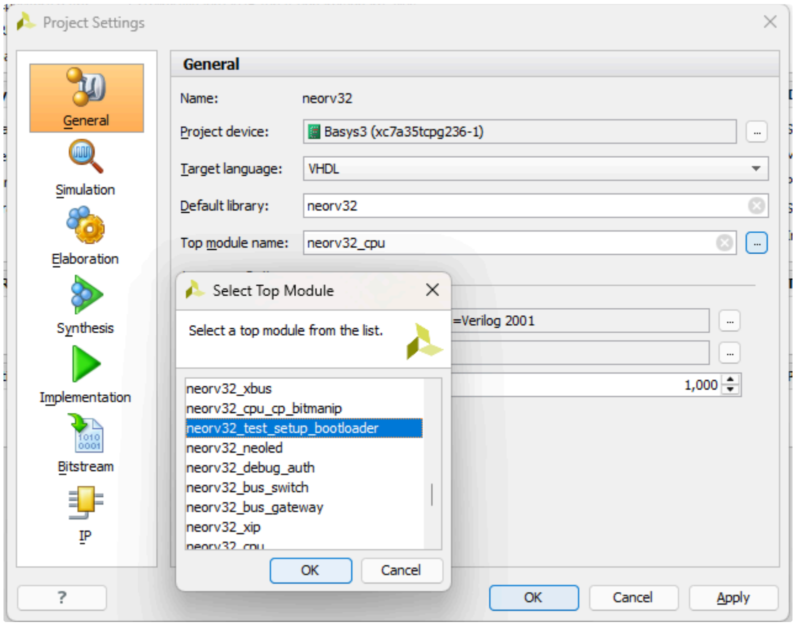
Status: Not started
Messages: No errors or warnings
Part: xc7z010clg400-1
Strategy: Vivado Implementation Defaults

Tcl Console

```
INFO: [IP_Flow 19-1704] No user IP repositories specified
INFO: [IP_Flow 19-2313] Loaded Vivado IP repository '/opt/Xilinx/Vivado/2016.4/data/ip'.
set_property board_part digilentinc.com:zybo-z7-10:part0:1.1 [current_project]
set_property target_language VHDL [current_project]
add_files -scan_for_includes {/home/fretz/wsp/neorv32/rtl/core /home/fretz/wsp/neorv32/rtl/test_setups/neorv32_test_setup_bootloader.vhd}
import_files -force
INFO: [filemgmt 20-348] Importing the appropriate files for fileset: 'sources_1'
import_files -fileset constrs_1 -force -norecurse /home/fretz/wsp/Downloads/digilent-xdc-master/Zybo-Z7-Master.xdc
set_property default_lib neorv32 [current_project]
```

Configure synthesis, simulation, implementation and IP related options

- Rename the Default library `xil_defaultlib` with `neorv32` and choose as top module name the `neorv32_test_setup_bootloader`. Close the Project Settings by pressing the Apply and OK buttons



General

Name: neorv32
Project device: Basys3 (xc7a35tcpg236-1)
Target language: VHDL
Default library: neorv32
Top module name: neorv32_cpu
=Verilog 2001
1,000

Select Top Module

Select a top module from the list.

- neorv32_xbus
- neorv32_cpu_cp_bitmanip
- neorv32_test_setup_bootloader
- neorv32_neoled
- neorv32_debug_auth
- neorv32_bus_switch
- neorv32_bus_gateway
- neorv32_xip
- neorv32_cpu

OK Cancel

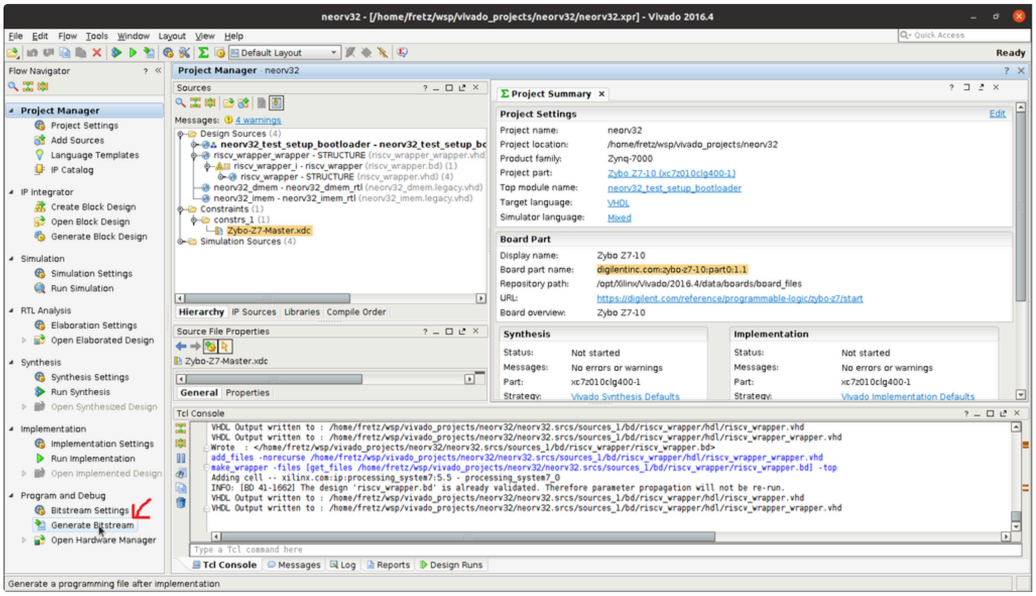
- Open the XDC file of the board to connect the NEORV32 ports to the appropriate pins of the FPGA.
- You should modify the following pins.

```
## This file is a general .xdc for the Basys3 rev B board
## To use it in a project:
## - uncomment the lines corresponding to used pins
## - rename the used ports (in each line, after get_ports) according to the top level signal names in the project
# Clock signal
set_property -dict { PACKAGE_PIN W5   IOSTANDARD LVCMOS33 } [get_ports clk_i]
create_clock -add -name sys_clk_pin -period 10.00 -waveform {0 5} [get_ports clk_i]
## Switches
set_property -dict { PACKAGE_PIN R2    IOSTANDARD LVCMOS33 } [get_ports {rstn_i}]
```

```
## LEDs
set_property -dict { PACKAGE_PIN U16   IOSTANDARD LVCMOS33 } [get_ports {gpio_o[0]}]
set_property -dict { PACKAGE_PIN E19   IOSTANDARD LVCMOS33 } [get_ports {gpio_o[1]}]
set_property -dict { PACKAGE_PIN U19   IOSTANDARD LVCMOS33 } [get_ports {gpio_o[2]}]
set_property -dict { PACKAGE_PIN V19   IOSTANDARD LVCMOS33 } [get_ports {gpio_o[3]}]
set_property -dict { PACKAGE_PIN W18   IOSTANDARD LVCMOS33 } [get_ports {gpio_o[4]}]
set_property -dict { PACKAGE_PIN U15   IOSTANDARD LVCMOS33 } [get_ports {gpio_o[5]}]
set_property -dict { PACKAGE_PIN U14   IOSTANDARD LVCMOS33 } [get_ports {gpio_o[6]}]
set_property -dict { PACKAGE_PIN V14   IOSTANDARD LVCMOS33 } [get_ports {gpio_o[7]}]
#USB-RS232 Interface
set_property -dict { PACKAGE_PIN B18   IOSTANDARD LVCMOS33 } [get_ports get_ports uart0_rxd_i]
set_property -dict { PACKAGE_PIN A18   IOSTANDARD LVCMOS33 } [get_ports uart0_txd_o]
## Configuration options, can be used for all designs
set_property CONFIG_VOLTAGE 3.3 [current_design]
set_property CFGBVS VCCO [current_design]
## SPI configuration mode options for QSPI boot, can be used for all designs
set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
set_property BITSTREAM.CONFIG.CONFIGRATE 33 [current_design]
set_property CONFIG_MODE SPIx4 [current_design]
```

Attention: The reset pin of the processor is connected to SW[15]. The reset pin is global reset, **low-active**, async, so the SW[15] should be on the ON position.

- Save the XDC file and press the Generate Bitstream button. This will generate the bitstream after synthesis and implementation are successfully finished.



neorv32 - [/home/fretz/wsp/vivado_projects/neorv32/neorv32.xpr] - Vivado 2016.4

Project Settings
Project name: neorv32
Project location: /home/fretz/wsp/vivado_projects/neorv32
Product family: Zynq-7000
Project part: Zybo Z7-10 (xc7z010clg400-1)
Top module name: neorv32_test_setup_bootloader
Target language: VHDL
Simulator language: Mixed

Board Part
Display name: Zybo Z7-10
Board part name: digilentinc.com:zybo-z7-10:part0:1.1
Repository path: /opt/Xilinx/Vivado/2016.4/data/boards/board_files
URL: https://digilent.com/reference/programmable-logic/zybo-z7/start
Board overview: Zybo Z7-10

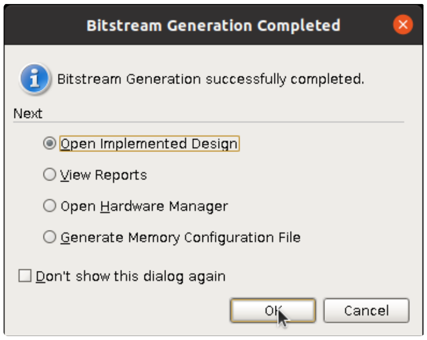
Synthesis
Status: Not started
Messages: No errors or warnings
Part: xc7z010clg400-1
Strategy: Vivado Synthesis Defaults

Implementation
Status: Not started
Messages: No errors or warnings
Part: xc7z010clg400-1
Strategy: Vivado Implementation Defaults

```
VHDL Output written to : /home/fretz/wsp/vivado_projects/neorv32/neorv32.srcs/sources_1/bd/riscv_wrapper/hdl/riscv_wrapper.vhd
VHDL Output written to : /home/fretz/wsp/vivado_projects/neorv32/neorv32.srcs/sources_1/bd/riscv_wrapper/hdl/riscv_wrapper_wrapper.vhd
Wrote  : </home/fretz/wsp/vivado_projects/neorv32/neorv32.srcs/sources_1/bd/riscv_wrapper/riscv_wrapper.bd>
add_files -norecurse /home/fretz/wsp/vivado_projects/neorv32/neorv32.srcs/sources_1/bd/riscv_wrapper/hdl/riscv_wrapper_wrapper.vhd
make_wrapper -files [get_files /home/fretz/wsp/vivado_projects/neorv32/neorv32.srcs/sources_1/bd/riscv_wrapper/riscv_wrapper.bd] -top
Adding cell -- xilinx.com:ip:processing_system7:5.5 - processing_system7_0
INFO: [BD 41-1662] The design 'riscv_wrapper.bd' is already validated. Therefore parameter propagation will not be re-run.
VHDL Output written to : /home/fretz/wsp/vivado_projects/neorv32/neorv32.srcs/sources_1/bd/riscv_wrapper/hdl/riscv_wrapper.vhd
VHDL Output written to : /home/fretz/wsp/vivado_projects/neorv32/neorv32.srcs/sources_1/bd/riscv_wrapper/hdl/riscv_wrapper_wrapper.vhd
```

Generate a programming file after implementation

- When the bitstream generation finishes, open to see the implemented design



Bitstream Generation Completed

Bitstream Generation successfully completed.

Next

● Open Implemented Design

○ View Reports

○ Open Hardware Manager

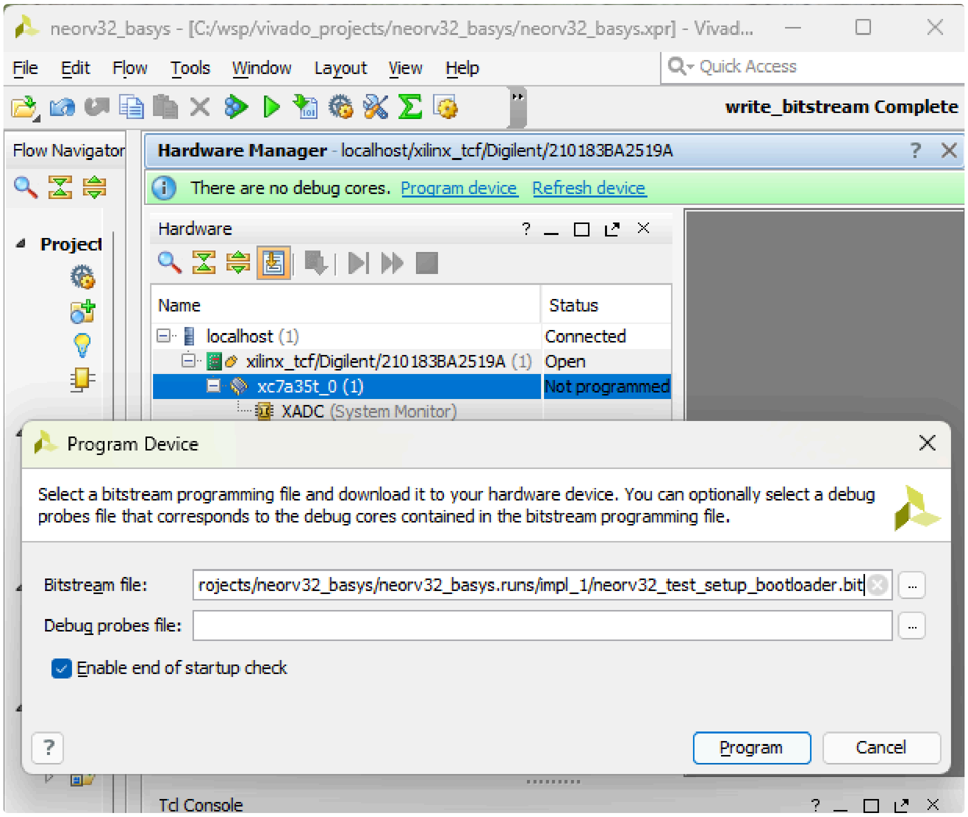
○ Generate Memory Configuration File

□ Don't show this dialog again

OK Cancel

Board setup and run Hello World software on the NEORV-32

- Open Hardware Manager and program the FPGA



neorv32_basys - [C:/wsp/vivado_projects/neorv32_basys/neorv32_basys.xpr] - Vivad...

write_bitstream Complete

Hardware Manager - localhost/xilinx_tcf/Digilent/210183BA2519A

There are no debug cores. Program device Refresh device

Name	Status
localhost (1)	Connected
xilinx_tcf/Digilent/210183BA2519A (1)	Open
xc7a35t_0 (1)	Not programmed
XADC (System Monitor)	

Program Device

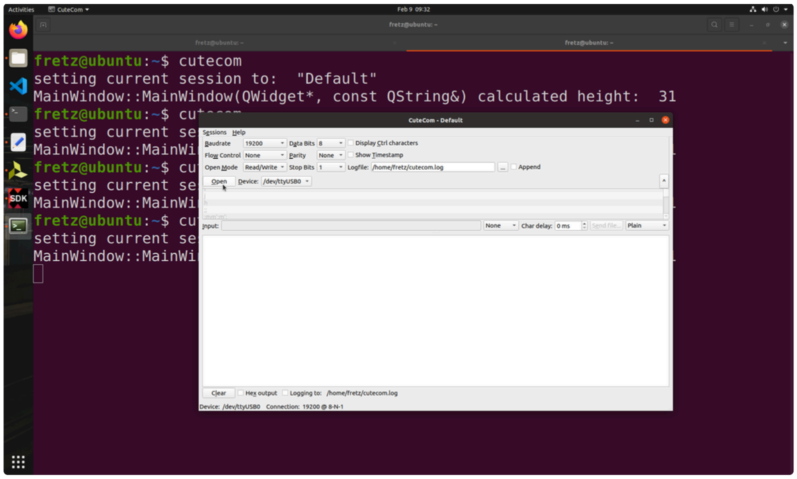
Select a bitstream programming file and download it to your hardware device. You can optionally select a debug probes file that corresponds to the debug cores contained in the bitstream programming file.

Bitstream file: rojects/neorv32_basys/neorv32_basys.runs/impl_1/neorv32_test_setup_bootloader.bit

Debug probes file:

☑ Enable end of startup check

- Once you program the FPGA you should see that the LD0 blinks (left side of the photo) after you press the reset button. Also, the DONE led should be ON.
- Open a terminal and press `cutecom`
  - In windows use HTerm
- Click on settings and configure as follows and then click on open



```
fretz@ubuntu:~$ cutecom
setting current session to:  "Default"
MainWindow::MainWindow(QWidget*, const QString&) calculated height:  31
fretz@ubuntu:~$ cu
setting current se
MainWindow::MainWi
fretz@ubuntu:~$ cu
setting current se
MainWindow::MainWi
fretz@ubuntu:~$ cu
setting current se
MainWindow::MainWi
```

CuteCom - Default

Baudrate 19200 Data Bits 8 □ Display Ctrl characters

Flow Control None Parity None □ Show Timestamp

Open Mode Read/Write Stop Bits 1 Logfile: /home/fretz/cutecom.log □ Append

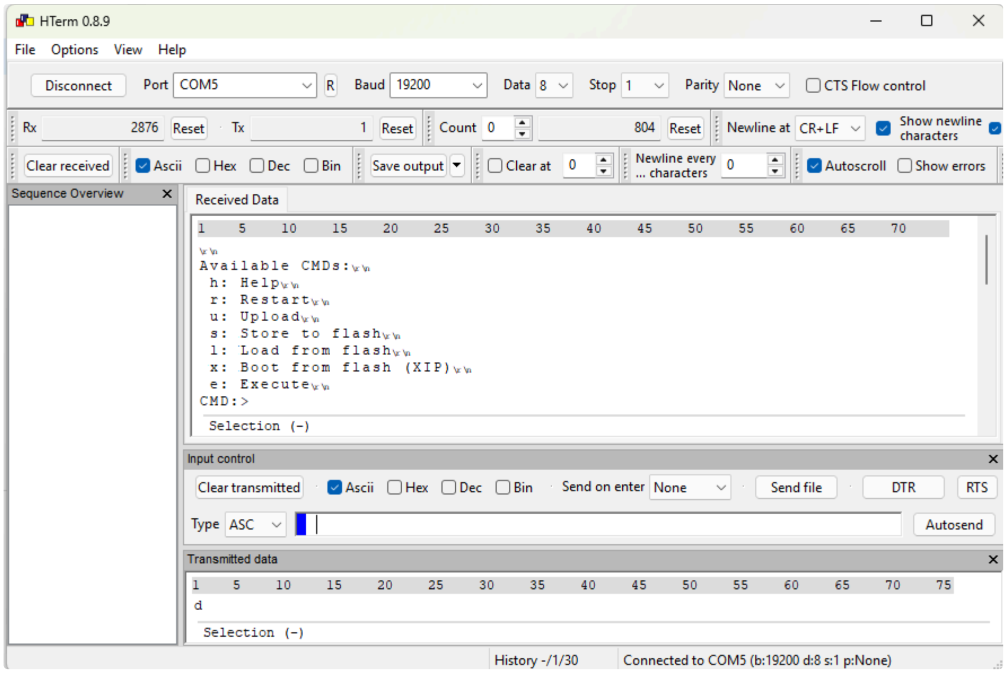
Device: /dev/ttyUSB0

Input: None Char delay: 0 ms Plain

□ Hex output □ Logging to: /home/fretz/cutecom.log

Device: /dev/ttyUSB0 Connection: 19200 @ 8-N-1

- For HTerm in MS windows, see below



HTerm 0.8.9

Disconnect | Port COM5 | Baud 19200 | Data 8 | Stop 1 | Parity None | □ CTS Flow control

Rx 2876 | Tx 1 | Count 0 | 804 | Newline at CR+LF | ☑ Show newline characters

☑ Ascii □ Hex □ Dec □ Bin | □ Clear at 0 | Newline every ... characters 0 | ☑ Autoscroll □ Show errors

Received Data

```
\r\n
Available CMDs:\r\n
 h: Help\r\n
 r: Restart\r\n
 u: Upload\r\n
 s: Store to flash\r\n
 l: Load from flash\r\n
 x: Boot from flash (XIP)\r\n
 e: Execute\r\n
CMD:>
```

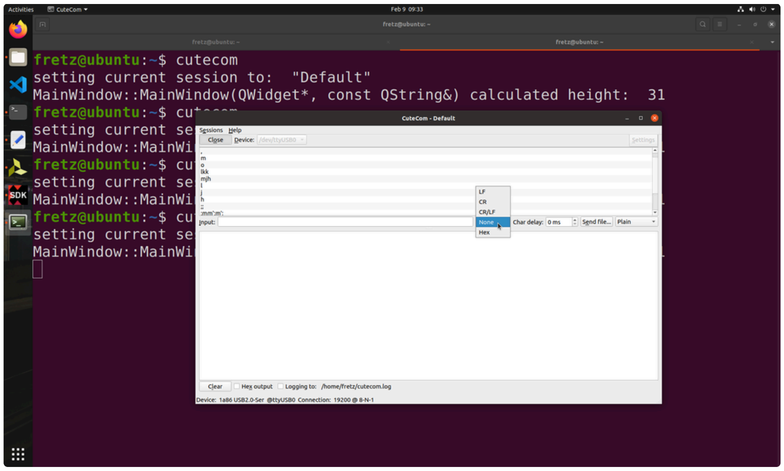
Input control: ☑ Ascii □ Hex □ Dec □ Bin | Send on enter None | Type ASC

Transmitted data

```
d
```

History -/1/30 | Connected to COM5 (b:19200 d:8 s:1 p:None)

Select None



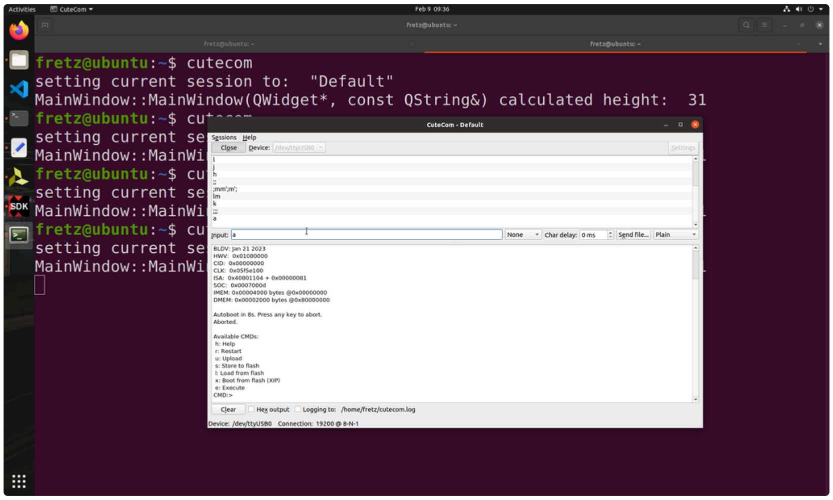
```
fretz@ubuntu:~$ cutecom
setting current session to:  "Default"
MainWindow::MainWindow(QWidget*, const QString&) calculated height:  31
```

CuteCom - Default

Device: /dev/ttyUSB0 | Input: | None | Char delay: 0 ms | Send file... | Plain

Device: 1a86 USB2.0-Ser @ttyUSB0 Connection: 19200 @ 8-N-1

- In the input, add the character `a`, press the reset button of NEORV32-V on the board and then press enter on cutecom.



```
fretz@ubuntu:~$ cutecom
setting current session to:  "Default"
MainWindow::MainWindow(QWidget*, const QString&) calculated height:  31
```

CuteCom - Default

Device: /dev/ttyUSB0 | Input: a | None | Char delay: 0 ms | Send file... | Plain

```
BLDV: Jan 21 2023
HWV:  0x01080000
CID:  0x00000000
CLK:  0x05f5e100
ISA:  0x40801104 + 0x00000081
SOC:  0x0007000d
IMEM: 0x00004000 bytes @0x00000000
DMEM: 0x00002000 bytes @0x80000000

Autoboot in 8s. Press any key to abort.
Aborted.

Available CMDs:
 h: Help
 r: Restart
 u: Upload
 s: Store to flash
 l: Load from flash
 x: Boot from flash (XIP)
 e: Execute
CMD:>
```

Logging to: /home/fretz/cutecom.log

Device: /dev/ttyUSB0 Connection: 19200 @ 8-N-1

Continue from here: Compile your first hello world example!!!!

- Let's download some application examples. Open a terminal and type

```
cd ~/wsp/neorv32/sw/example
make clean_all
make all
```

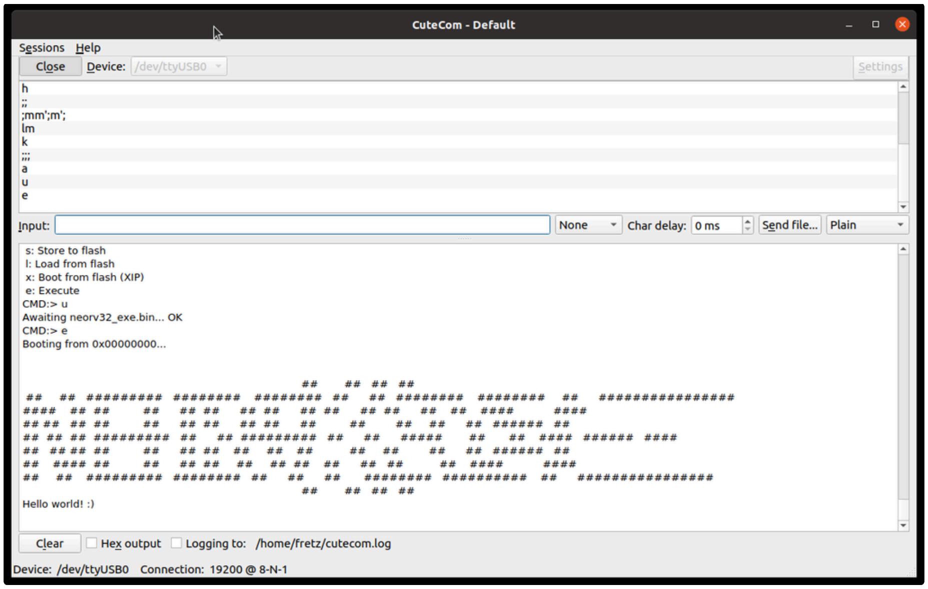
- On cutecome enter the character `u` and press enter

```
CMD:> u
Awaiting neorv32_exe.bin...
```

- On cutecome click the send file button
- If everything goes fine, OK will appear in your terminal:

```
CMD:> u
Awaiting neorv32_exe.bin... OK
```

- The executable is now in the instruction memory of the processor. To execute the program right now, run the "Execute" command by typing `e` in cutecome and press the Enter on your keyboard:



```
h
;;
;mm';m';
lm
k
;;;
a
u
e
```

```
 s: Store to flash
 l: Load from flash
 x: Boot from flash (XIP)
 e: Execute
CMD:> u
Awaiting neorv32_exe.bin... OK
CMD:> e
Booting from 0x00000000...


                                                                       ##        ##   ##   ##
 ##     ##   #########   ########    ########   ##      ##   ########    ########     ##   ################
####    ##  ##          ##      ##  ##      ##  ##      ##  ##      ##  ##      ##   ##  ####            ####
## ##   ##  ##          ##      ##  ##      ##  ##      ##          ##         ##    ##    ##   ######   ##
##  ##  ##  #########   ##      ##  #########   ##      ##      #####        ##      ##  ####   ######   ####
##   ## ##  ##          ##      ##  ##    ##     ##    ##           ##     ##        ##    ##   ######   ##
##    ####  ##          ##      ##  ##     ##     ##  ##    ##      ##   ##          ##  ####            ####
##     ##   #########    ########   ##      ##      ##       ########   ##########   ##    ################
                                                                       ##        ##   ##   ##
Hello world! :)
```

Device: /dev/ttyUSB0 Connection: 19200 @ 8-N-1