VHDL Coding Examples – Part1: Combinational Circuits

Tuesday 14 November, 2023

1. Write VHDL models that implement the two following functions using concurrent signal assignment.

   a) F(A,B) = A'*B + A + A*B'

   b) F(A;B;C;D) = A'*C*D' + B'*C + B*C*D'

2. Provide a VHDL model of an 8:1 MUX (multiplexer) using conditional signal assignment (when-else)

3. Write VHDL models that implement the two following functions using sequential signal assignment (if-else) statements.

   a) F(A,B) = A'*B + A + A*B'

   b) F(A;B;C;D) = A'*C*D' + B'*C + B*C*D'

4. Provide a VHDL model of an 8:1 MUX (multiplexer) using sequential signal assignment (if-else) statements.

5. Provide a VHDL model of an 8:1 MUX (multiplexer) using sequential signal assignments (case & if-else) statements. The multiplexer must have a circuit enable (CE) signal .When CE = '1', the mux works properly. When CE is '0', the output of the MUX is '0'.

Attention:

- ☑ Submission Deadline: **21 November 2023**.
- ☑ Upload your report (pdf file) in gunet platform