### **RISC-V** tutorial

This tutorial will guide you to implement the RISC-V "neorv32" processor on the Zybo Z7 board and set the RISC-V compiler toolchain on Ubuntu.



You can find additional information for the NEORV-32 microarchitecture in the following links

- [Datasheet] The NEORV32 RISC-V Processor
- [User Guide] The NEORV32 RISC-V Processor
- https://github.com/stnolting/neorv32/tree/v1.7.2 Can't find link

### Hardware implementation

- First, we should download the VHDL source code of the NEORV-32.
- Open a terminal and type the following:
- 1 cd
- 2 mkdir -p wsp
- 3 cd wsp
- 4 git clone https://github.com/stnolting/neorv32.git
- 5 cd neorv32/
- 6 git checkout v1.8.0
- · Beautiful, we now have the source code for NEORV-32. Let's open Vivado to implement the processor
- Open Vivado

```
1 cd
2 cd wsp
3 mkdir -p vivado_projects
4 cd vivado_projects
```

5 source /opt/Xilinx/Vivado/2016.4/settings64.sh

```
6 vivado &
```

• Create a new project. Click from Vivado menu File  $\rightarrow$  New project and click on the next button



• Type neorv32 as the project name

| New Project   | ×    |
|---|------|
| Project Name<br>Enter a name for your project and specify a directory where the project<br>data files will be stored. |      |
| Project name: neorv32   | 8    |
| Project location: /home/fretz/wsp/vivado_projects   | ×    |
| Create project subdirectory   |      |
| Project will be created at: /home/fretz/wsp/vivado_projects/neorv32   |      |
| ? <u>Back</u> <u>N</u> ext > <u>Finish</u> Ca   | ncel |

Choose the RTL project



- Choose as target language VHDL and click on the Add Directories button to add the VHDL source code of the NEORV-32
- Choose the Directory → /home/fretz/wsp/neorv32/rtl/core/

| Add Source Directories  |        |            | ×     |
|---|--------|------------|-------|
| Recent: 🖻 /home/fretz/wsp/vivado_projects 🔹 🔹 🚳   | AX     | 2          | 25    |
| Directory: /home/fretz/wsp/neorv32/rtl/core   |        |            |       |
| <pre>     cdrom     dev     dev     etc     bosktop     Documents     Downloads     Snap     meorv32     docs     neorv32     docs     rtl     fret_core     mem     processor_templates     system_integration     fret_setups     sim     sw     old     rivado_projects     men/2 </pre> |        |            |       |
|   | Select | ) <b>C</b> | ancel |

• Click on the Add Files button to add one more source code. Choose

.

/home/fretz/wsp/neorv32/rtl/test\_setups/neorv32\_test\_setup\_bootloader.vhd and click on the OK button

|   | Add Source Files 🛛 😵  |
|---|---|
| Look in: Look in: test_setup_approm.vhd<br>neorv32_test_setup_bootloader.vhd<br>neorv32_test_setup_on_chip_debugger.vhd | Image: Solution of source code must retain the conditions of source code must retain the conditions and the following disclaimer. |
| File <u>n</u> ame: neorv32_test_setup_approm.vhd  |   |
| Files of type: Design Source Files (.vhd, vhdl, vhf,  | vhdp, vho, v, vf, verilog, vr, vg, vb, tf, vlog, vp, vm, veo, vh, h, svh, vh  |
|   | OK Cancel   |

• Tick the Scan and add RTL include files into the project, and finally click on the NEXT button

|                                 | New Proj   | ect                                |   | 8        |  |  |
|---------------------------------|--|------------------------------------|---|----------|--|--|
| Add Sources                     |  |                                    |   |          |  |  |
| Specify HDL a<br>to your projec | nd netlist files, or directories contair<br>ct. Create a new source file on disk a | hing HDL and r<br>and add it to ye | netlist files, to add<br>our project. You can |          |  |  |
| ▲ Index                         | Name   | Library                            | HDL Source For                                |          |  |  |
| <b>1</b>                        | core   | xil_defaultlib                     | Synthesis & Simulation                        | 1 🔻 /hor |  |  |
| - 🕑 2                           | neorv32_test_setup_bootloader.vhd  | xil_defaultlib                     | Synthesis & Simulation                        | n 🔻 /hor |  |  |
| •                               | Add Files Add Directo  | ries <u>C</u>                      | reate File                                    | Þ        |  |  |
| 📈 Scan and add                  | d RTL include files into project   |                                    |   |          |  |  |
| Copy <u>s</u> ources            | into project   |                                    |   |          |  |  |
| Add sources f                   | Add sources from subdirectories  |                                    |   |          |  |  |
| Target language                 | *: VHDL 👻 Simulator language   | e: Mixed 🔻                         |   |          |  |  |
| ?                               | < <u>B</u> a   | ick <u>N</u> ext :                 | > <u>F</u> inish C                            | ancel    |  |  |

#### Click next on the Add Existing IP (optional)

| New Project   | ×   |
|---|-----|
| Add Existing IP (optional)<br>Specify existing configurable IP, DSP composite, and Embedded sub-design files to<br>add to your project. |     |
| Use Add Files or Add Directories buttons below  |     |
| Add Files Add Directories   |     |
| ? Einish Can  | cel |

Click on the Add Files on the Add Constraints window

| New Project   | 8        |
|---|----------|
| Add Constraints (optional)<br>Specify or create constraint files for physical and timing constraints. | <b>~</b> |
| Use Add Files or Create File buttons below  |          |
| Add Nes Create File   |          |
| ?EackEinish   | Cancel   |

• Choose the /home/fretz/wsp/Downloads/digilent-xdc-master/Zybo-Z7-Master.xdc and press the OK button

| Add Const                                      | raint Files 🛛 😣  |
|--|--|
| Look <u>i</u> n: 📁 digilent-xdc-master         | 💽 🤌 🗐 🖉 🔌 🗐 🖃  |
| Arty-A7-35-Master.xdc                          | Recent Directories   |
| 🗈 Arty-A7-100-Master.xdc 🛛 🚹 Zybo-Master.xdc   | home/fretz/wsp/neory32/rtl/test_setups   |
| Arty-Master.xdc 🚹 Zy p-Z7-Master.xdc           | File Dreview   |
| Arty-S7-25-Master.xdc                          |  |
| Arty-S7-50-Master.xdc                          | ## This file is a general .xdc for the Zybo Z7 Rev. B  |
| Arty-Z7-10-Master.xdc                          | ## To use it in a project:   |
| Arty-Z7-20-Master.xdc                          | ## - uncomment the lines corresponding to used pins  |
| Basys-3-Master.xdc                             | ## - rename the used ports (in each line, after get_por  |
| Crood-A7-Master.xdc                            |  |
| Crood-S7-25-Master.xdc                         | ##CLOCK SIGNAL<br>#set property -dict { PACKAGE PIN K17 TOSTANDARD / VCN   |
| Cora-27-07S-Master.xdc                         | #create_clock -add -name sys_clk_pin -period 8.00 -wave  |
| Cora-27-10-Master.xdc                          |  |
| Eciypse-27-Master.xdc     Ganasys 2 Master.yds | ##Oritobaa   |
| Genesys-2-Master.xdc     Genesys-2-Master.xdc  | #set property -dict { PACKAGE PIN G15 TOSTANDARD / VCN   |
| Genesys-ZU-SEG-Master xdc                      | #set_property -dict { PACKAGE_PIN P15 IOSTANDARD LVCN  |
| Genesys-ZU-5EV-D-Master.xdc                    | #set_property -dict { PACKAGE_PIN W13 IOSTANDARD LVC   |
|  | #set_property -dict { PACKAGE_PIN T16 IOSTANDARD LVCN  |
| Nexys-4-DDR-Master.xdc                         |  |
| Nexys-4-Master.xdc                             | ##Buttons  |
| Nexys-A7-50T-Master.xdc                        | #set_property -dict { PACKAGE_PIN K18 IOSTANDARD LVCN  |
| Nexys-A7-100T-Master.xdc                       | #set_property -dict { PACKAGE_PIN_P16 IOSTANDARD LVCN  |
| Nexys-Video-Master.xdc                         | #set property -dict { PACKAGE_PIN_KI9 IUSTANDARD LVCF<br>#set property -dict { PACKAGE PIN_YI6 _ TOSTANDARD LVCF |
| README.md                                      |  |
| Sword-Master.xdc                               | V  |
| USB104-A7-100T-Master.xdc                      |  |
|  |  |
| File name: [Zybo-Z7-Master.xdc                 |  |
| Files of type: All Files                       |  |
|  |  |
|  | OK Cancel  |
|  |  |

- Tick the copy constraints files into project and click the Next button

| New Project  | 8        |
|--|----------|
| Add Constraints (optional)   |          |
| Specify or create constraint files for physical and timing constraints.                      | <u>-</u> |
| Constraint File Location<br>Zybo-Z7-Master.xdc /home/fretz/wsp/Downloads/digilent-xdc-master |          |
| Add Files Create File  |          |
| ? <u>A Back</u> <u>Next</u> > <u>Finish</u> Car  | cel      |

Click on Boards

| New Project                |                  |               |                    |                 | ×                     |                    |                   |                 |     |
|----------------------------|------------------|---------------|--------------------|-----------------|-----------------------|--------------------|-------------------|-----------------|-----|
| Default Part               |                  |               |                    |                 |                       |                    |                   |                 |     |
| Choose a default X         | (ilinx part or   | board for y   | our project.       | This can be     | changed later         |                    |                   |                 |     |
| Select: <mark> </mark>     | Blerds           |               |                    |                 |                       |                    |                   |                 |     |
| Produ <u>c</u> t category: | All              | -             | Spee <u>d</u> grad | le: All         | -                     |                    |                   |                 |     |
| <u>E</u> amily:            | All              | -             | <u>T</u> emp grade | e: All          | -                     |                    |                   |                 |     |
| <u>P</u> acka <b>ge</b> :  | All              | -             |                    |                 |                       |                    |                   |                 |     |
|                            |                  |               |                    | Reset All Filte | ers                   |                    |                   |                 |     |
| <u>S</u> earch: Q-         |                  |               | -                  |                 |                       |                    |                   |                 |     |
| Part                       | I/O Pin<br>Count | Block<br>RAMs | DSPs               | FlipFlops       | GTXE2<br>Transceivers | Gb<br>Transceivers | Available<br>IOBs | LUT<br>Elements |     |
| 🔷 xc7z010clg400-1          | 400              | 60            | 80                 | 35200           | 0                     | 0                  | 100               | 17600           | 2 🔺 |
| xc7z010iclg225-1L          | 225              | 60            | 80                 | 35200           | 0                     | 0                  | 54                | 17600           | 2   |
| 🔷 xc7z010iclg400-1L        | 400              | 60            | 80                 | 35200           | 0                     | 0                  | 100               | 17600           | 2   |
| 🔷 xc7z012sclg485-2         | 485              | 72            | 120                | 68800           | 0                     | 4                  | 150               | 34400           | 3   |
| 🔷 xc7z012sclg485-1         | 485              | 72            | 120                | 68800           | 0                     | 4                  | 150               | 34400           | 3   |
| 🔷 xc7z014sclg400-2         | 400              | 107           | 170                | 81200           | 0                     | 0                  | 125               | 40600           | 4   |
| 🔷 xc7z014sclg400-1         | 400              | 107           | 170                | 81200           | 0                     | 0                  | 125               | 40600           | 4   |
| 🔷 xc7z014sclg484-2         | 484              | 107           | 170                | 81200           | 0                     | 0                  | 200               | 40600           | 4   |
| 🔷 xc7z014sclg484-1         | 484              | 107           | 170                | 81200           | 0                     | 0                  | 200               | 40600           | 4   |
| 🔷 xc7z015clg485-3          | 485              | 95            | 160                | 92400           | 0                     | 4                  | 150               | 46200           | 3   |
| 🔷 xc7z015clg485-2          | 485              | 95            | 160                | 92400           | 0                     | 4                  | 150               | 46200           | 3   |
| 🔷 xc7z015clg485-1          | 485              | 95            | 160                | 92400           | 0                     | 4                  | 150               | 46200           | 3   |
| 🔷 xc7z015iclg485-1L        | 485              | 95            | 160                | 92400           | 0                     | 4                  | 150               | 46200           | 3 🖵 |
| 1                          |                  |               |                    |                 |                       |                    |                   |                 | ▶   |
| ?                          |                  |               |                    |                 | < <u>B</u> ack        | Next >             | <u> </u>          | Can             | cel |

Choose Zybo Z7-10 and press the next button

| New Project                                       |                   |             |                    | 8              |              |
|---|-------------------|-------------|--------------------|----------------|--------------|
| Default Part                                      |                   |             |                    |                |              |
| Choose a default Xilinx part or board for your pr | oject. This can b | e changed l | ater.              |                |              |
|   |                   |             |                    |                |              |
| Select: 🚸 Parts 📓 Boards                          |                   |             |                    |                |              |
| # Filter/ Preview                                 |                   |             |                    |                |              |
| Vendor: All 🗸                                     |                   |             |                    |                |              |
| Display Name: All                                 |                   |             |                    |                |              |
|   |                   |             |                    |                |              |
| Board Rev: Latest                                 |                   |             |                    |                |              |
| Reset All Filters                                 |                   |             |                    |                |              |
| Search: Q-  | -                 |             |                    |                |              |
|   |                   |             |                    |                |              |
| Display Name                                      | Vendor            | Board Rev   | Part               | I/O Pin Count  | File Versior |
| Arty Z7-10  | digilentinc.com   | A.0         | xc7z010clg400-1    | 400            | 1.1          |
| Arty Z7-20  | digilentinc.com   | A.0         | xc7z020clg400-1    | 400            | 1.1          |
| 📓 Cora Z7-07S                                     | digilentinc.com   | B.0         | 🔷 xc7z007sclg400-1 | 400            | 1.1          |
| 📓 Cora Z7-10                                      | digilentinc.com   | B.0         | 🔷 xc7z010clg400-1  | 400            | 1.1          |
| 📓 Eclypse Z7                                      | digilentinc.com   | B.0         | 🔷 xc7z020clg484-1  | 484            | 1.1          |
| Zedboard  | digilentinc.com   | D.3         | 🔷 xc7z020clg484-1  | 484            | 1.1          |
| 📓 Zybo Z 🔊 10                                     | digilentinc.com   | B.2         | 📎 xc7z010clg400-1  | 400            | 1.1          |
| 📓 Zybo Z7-20                                      | digilentinc.com   | B.2         | 🔷 xc7z020clg400-1  | 400            | 1.1          |
| 🖉 Zybo  | digilentinc.com   | B.4         | xc7z010clg400-1    | 400            | 2.0          |
| ZedBoard Zyng Evaluation and Development Kit      | em.avnet.com      | d           | xc7z020clg484-1    | 484            | 1.3          |
| ZYNQ-7 ZC702 Evaluation Board                     | xilinx.com        | 1.0         | xc7z020clg484-1    | 484            | 1.2          |
|   |                   |             | Ť                  |                |              |
|   |                   |             |                    |                |              |
|   |                   |             |                    |                | Þ            |
| ?   |                   | < <u>E</u>  | ack <u>N</u> ext > | <u>F</u> inish | Cancel       |

• Finally, click on the Finish button

|                               | New Project 🛛 😵  |
|-------------------------------|--|
|                               | New Project Summary  |
| HLx Editions                  | () A new RTL project named 'neorv32' will be created.  |
|                               | ① 1 source file will be added.   |
|                               | 1 source directory will be added.  |
|                               | 🛦 No Configurable IP files will be added. Use Add Sources to add them later.   |
|                               | ① 1 constraints file will be added.  |
|                               | <ul> <li>The default part and product family for the new project:<br/>Default Board: Zybo Z7-10<br/>Default Part: xcZ010clg400-1<br/>Product: Zynq-7000<br/>Family: Zynq-7000<br/>Package: clg400<br/>Speed Grade: -1</li> </ul> |
| E XILINX<br>ALL PROGRAMMABLE. | To create the project, click Finish  |
| ?                             | < <u>B</u> ack Next > <b>N</b> ext > Cancel Cancel   |

• Select the Project Settings under the Project Manager

|   | neorv32 - [/home/fretz/v   | vsp/vivado_projects/neorv32/neorv32.xpr] - Vivado 2016.4  | ہ – ۳ 😣                                  |  |  |  |  |
|---|--|---|--|--|--|--|--|
| ile <u>E</u> dit Flow <u>T</u> ools <u>W</u> indow La           | Yout Yiew Help   |   | Q. • Quick Access                        |  |  |  |  |
| 2) 🖙 🕫 🎼 🏗 🗙 👂 🕨 😫 🤅  | 🕽 🐝 🔽 🚳 🖾 Default Layout 🛛 👻 🔭 🔍 🧐   |   | Ready                                    |  |  |  |  |
| low Navigator ? «   | Project Manager - neorv32  |   | ? ×                                      |  |  |  |  |
| 人間章   | Sources ? = 🗆 🛃 ×  | E Project Summary ×   | ? 🗆 🕹 ×                                  |  |  |  |  |
| Project Manager 🥜   | <ul> <li>또 (#) (#) (전 1) (#) (전 1)</li> </ul>  | Project Settings  | Edit                                     |  |  |  |  |
| Prefect Settings  | Messages: () <u>6 warnings</u>   | Project name: neorv32   |  |  |  |  |  |
| add Sources   | o-@4 neorv32_test_setup_bootloader - neorv32_tes   | Project location: /home/fretz/wsp/vivado_projects/neor  | rv32                                     |  |  |  |  |
| Language Templates     IR Catalog                               | neorv32_dmem - neorv32_dmem_rtl (neorv32_dmem.l<br>neorv32_imem - neorv32_imem_rtl (neorv32_imem.lec   | Product family: Zynq-7000 Project part: Zynq-7000   |  |  |  |  |  |
| - in Catalog  | e-Constraints (1)  | Top module name: neory32 test setup bootloader  |  |  |  |  |  |
| IP Integrator   | alliulation addres (3)   | Target language: VHDL   |  |  |  |  |  |
| Create Block Design     Open Plock Design                       |  | Simulator language: Mixed   |  |  |  |  |  |
| Generate Block Design   | 4  | Board Part  |  |  |  |  |  |
| Circulation   | Hierarchy Libraries Compile Order  | Display name: Zybo 27-10  |  |  |  |  |  |
| Simulation     Simulation Settings                              | Source File Properties ? _ D L* ×  | Board part name: digilentinc.com:zybo-z7-10:part0:1.1   |  |  |  |  |  |
| Run Simulation  |  | Repository path: /opt/Xilirw/Vivado/2016.4/data/boards/b  | pard_files                               |  |  |  |  |
| DTI Anohoio   | e neorv32_bootidader_image.vnd   | URL: https://digilent.com/reference/program<br>Reard exercises 2/dep 27-10                                      | mable-logic/zybo-z7/start                |  |  |  |  |
| RTL Analysis     RTL Analysis     RTL Analysis     RTL Analysis | ☑ Enabled  | Solid delever. 2300 27-20   |  |  |  |  |  |
| Open Elaborated Design  | Location: /home/fretz/wsp/vivado_projects/neorv32,   | Synthesis   | Implementation                           |  |  |  |  |
| Sunthesis   | Type: VHDL -   | Status: Not started   | Status: Not started                      |  |  |  |  |
| Synthesis Settings  | Library: neorv32 -   | Part: xc7z010clg400-1   | Part: vc7z010cig400-1                    |  |  |  |  |
| Run Synthesis   | General Properties   | Strategy: Vivado Synthesis Defaults   | Strategy: Vivado Implementation Defaults |  |  |  |  |
| 👂 📄 Open Synthesized Design                                     | Tcl Console  | in the second | ? _ 🗆 🗷 ×                                |  |  |  |  |
| Implementation  | INFO: [IP_Flow 19-1704] No user IP repositories :  | specified   | -  |  |  |  |  |
| Implementation Settings   | In-U: [IP_Flow 19-2313] Loaded Vivado IP reposito<br>set_property board_part digilentinc.com:zybo-z7-1   | pry /opt/allink/Vivado/2016.4/data/ip'.<br>l0:part0:l.1 [current_project]                                       |  |  |  |  |  |
| Run Implementation  | <pre>set_property target_language VHDL [current_project add files -scan for includes {/home/fretz/wsp/nect</pre>   | ct]<br>prv32/rtl/core /home/fretz/vsp/neorv32/rtl/test setups/neo   | rv32 test setup bootloader.vhd)          |  |  |  |  |
| Open Implemented Design   | TNEO: [filement 20.249] Importing the appropriate  | files for fileset, 'sources l'  |  |  |  |  |  |
| Program and Debug   | Light C1NF0: [filesgat 20-348] Taporting the appropriate files for fileset: "sources] the sources of the so |   |  |  |  |  |  |
| Bitstream Settings  | <pre>set_property default_lib neorv32 [current_project</pre>   |   |  |  |  |  |  |
| Generate Bitstream  |  |   |  |  |  |  |  |
| Type a Tcl command Harney                                       |  |   |  |  |  |  |  |
| 🗏 Td Console 💿 Messages 🖾 Log 🔛 Reports 🐌 Design Runs           |  |   |  |  |  |  |  |
| onfigure synthesis, simulation, impler                          | mentation and IP related options   |   |  |  |  |  |  |

• Rename the Default library xil\_defaultlib with neorv32. Close the Project Settings by pressing the Apply and OK buttons

|  |  | Project Settings 🛛 😣  |
|--|--|---|
| General<br>General<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimulation<br>Gimula | General         Name:         Project device:         Target language:         Default library:         Top module name:         Language Options         Verilog options         Generics/Parar         Loop count: | Project Settings     neorv32   Zybo Z7-10 (xc7z010clg400-1)   HDL   neorv32   neorv32     neorv32     neorv32     neorv32     1,000 |
| istream<br>iP<br>iP  |  |   |
| ?  |  | OK Cancel Apply   |

#### Click on the Create Block Design

|   | neorv32 - [/home/fret   | z/wsp/vivado_projects/neorv32/neorv32.xpr] - Vivado 20   | 016.4                        |                                | a (           |
|---|---|--|------------------------------|--------------------------------|---------------|
| ile <u>E</u> dit Flow <u>T</u> ools <u>W</u> indow La | ayout Yiew Help   |  |                              | Q+ Quick Access                |               |
| 2) 🖙 🕫 🌇 🛍 🗙 👂 🕨 🐮 🤇                                  | 🖏 🐝 ∑ 🗔 🖂 Default Layout 🛛 👻 🔆 🔍  |  |                              |                                | Read          |
| low Navigator ? «                                     | Project Manager - neorv32   |  |                              |                                | ?             |
| 大国章   | Sources ? = D L <sup>2</sup> ?  | Σ Project Summary ×                                      |                              | ? [                            | o Ľ ×         |
| Project Manager                                       | a 🖾 🗰 📾 😹 🖩 💽   | Project Settings   |                              |                                | Edit          |
| Project Settings                                      | Messages: () <u>6 warnings</u>  | Project name: neorv32                                    |                              |                                | _             |
| 👌 Add Sources   |   | Project location: /home/fretz/wsp/vivado_projects/       | /neorv32                     |                                |               |
| 💡 Language Templates                                  | -@ neorv32_dmem - neorv32_dmem_rtl (neorv32_dme   | n.l Product family: Zynq-7000                            |                              |                                |               |
| 💷 IP Catalog  | meorv32_imem - neorv32_imem_rtl (neorv32_imem.  | eg Project part: <u>Zybo Z7-10 (xc7z010clg400-1)</u>     |                              |                                |               |
| IP Integrator   | erea Simulation Sources (3)   | Top module name: neorv32_test_setup_bootloader           |                              |                                |               |
| 🕂 Create Block Design 🝊                               |   | Target language: VHDL                                    |                              |                                |               |
| Doen Block Design                                     |   | Simulator language: Mixed                                |                              |                                |               |
| 6 Generate Black Design                               | 4   | Board Part   |                              |                                |               |
|   | Hierarchy Ubraries Compile Order  | Display name: Zybo 27-10                                 |                              |                                |               |
| Simulation  | Source File Properties ? - D C ?  | Board part name: digilentinc.com:zybo-z7-10:part0:1.     | 1                            |                                |               |
| Simulation Settings                                   | $\leftarrow \rightarrow \bigotimes \triangleright$  | Repository path: /opt/Xilinx/Vivado/2016.4/data/boar     | rds/board_files              |                                |               |
| e Run simulation                                      | eenv32_bootloader_image.vhd   | URL: https://digilent.com/reference/prog                 | grammable-logic/zybo-z7/star | ±                              |               |
| RTL Analysis  | 2 Enabled   | Board overview: Zybo Z7-10                               |                              |                                |               |
| 6 Elaboration Settings                                | Lessier fetetuntinde preistelesen (2)   | Synthesis  | Implementation               |                                |               |
| Open Elaborated Design                                | Time: VADI  | Status: Not started                                      | Status:                      | Not started                    |               |
| Synthesis   | Type: VHDL -  | Messages: No errors or warnings                          | Messages:                    | No errors or warnings          |               |
| Synthesis Settings                                    | Ubrary: neorv32 -   | Part: xc7z010clg400-1                                    | Part:                        | xc7z010clq400-1                |               |
| Run Synthesis   | General Properties  | Strategy: Vivado Synthesis Defaults                      | Strategy:                    | Vivado Implementation Defaults | 6             |
| 👂 📄 Open Synthesized Design                           | Tri Console   |  |                              | 2                              | <b>D</b> (2.) |
| Implementation  | INFO: [IP Flow 19-1704] No user IP repositorie  | s specified  |                              | r =                            |               |
| Implementation Settings                               | INFO: [IP_Flow 19-2313] Loaded Vivado IP report   | itory '/opt/Xilinx/Vivado/2016.4/data/ip'.               |                              |                                |               |
| Bun implementation                                    | set property board_part digitentinc.com:zybo-2  | iect]  |                              |                                |               |
| Open Implemented Design                               | add_files -scan_for_includes {/home/fretz/wsp/  | neorv32/rtl/core /home/fretz/wsp/neorv32/rtl/test_setups | /neorv32_test_setup_bootl    | oader.vhd}                     |               |
|   | INFO: [filengst 20-348] Importing the appropri  | ate files for fileset: 'sources_1'                       |                              |                                |               |
| Program and Debug                                     | import_files -fileset constrs_1 -force -norect<br>set presents default lib peers22 (success and | rse /home/fretz/wsp/Downloads/digilent-xdc-master/Zybo-Z | 7-Master.xdc                 |                                |               |
| Bitstream Settings                                    | sec_propercy denaucc_cro neorvaz (current_pro)  |  |                              |                                |               |
| Senerate bitstream                                    | 4   |  |                              |                                | •             |
| P av open nardware Manager                            | Type a Tcl command here   |  |                              |                                |               |
|   | 🗏 Tcl Console 🔎 Messages 🖾 Log 🍙 Reports 🦃  | Design Runs  |                              |                                |               |
| reate and add an IP subsystem to th                   | ne project  |  |                              |                                |               |

• Give the name riscv\_wrapper . Then press the OK button

|                      | Create Block Design                | 8      |
|----------------------|------------------------------------|--------|
| Please specify name  | 4                                  |        |
| <u>D</u> esign name: | riscv_wrapper                      | 8      |
| Directory:           | 🛜 <local project="" to=""></local> | *      |
| Specify source set:  | 🖻 Design Sources                   | -      |
|                      |                                    |        |
| ?                    | ОК                                 | Cancel |

· Create the following block design



· Next, create a VHDL wrapper for the block design



Select the Let Vivado manage and click the OK button



• Next, set as the top module the wrapper you just created

|   | neorv  | 32 - [/home/fretz/v  | vsp/vivado_project    | ts/neorv32  | /neorv32.xpr] - Vivado 2  | 016.4                               | _ σ  | 8      |
|---|--|----------------------|-----------------------|-------------|---|-------------------------------------|--|--------|
| ile Edit Flow Icols Window La               | ayout ⊻iew <u>H</u> elp  |                      |                       |             |   |                                     | Qr Quick Access  |        |
| 2) in 01 🕞 🎼 🗙 🔌 🎽 🔇                        | 🖏 🛞 🔽 🧑 🔤 Default Layout 🛛 🔹 🕽   | K 🕸 🖹 😜              |                       |             |   | Synth                               | esis and Implementation Out-of-date more                       | e info |
| low Navigator ? «                           | Project Manager - neorv32  |                      |                       |             |   |                                     |  | ? >    |
|   | Sources  | ? _ 🗆 🖻 X            | Deale et Cumm         |             |   |                                     | 2 🗆 12   | . ×    |
|   | 9, II (#) 😂 😹 (#) 🖲  |                      | L project Summ        | ary A       |   |                                     |  |        |
| Project Manager                             | Messages: () 4 warnings  |                      | Project Settings      | s           |   |                                     | Ed   | at     |
| Project Settings                            | O-Co Design Sources (4)  |                      | Project name:         | neo         | rv32  |                                     |  |        |
| Add Sources                                 | -@. neorv32_test_setup_bootlo  | ader - neorv32_tes   | Project location:     | /hor        | ne/fretz/wsp/vivado_projects  | s/neorv32                           |  | - 1    |
| Language Templates                          | meory32 dmem - neory32 dmen  | Source Node Pri      | operties              | Ctr/HE      | -7000   |                                     |  |        |
| 9- IP Catalog                               | neorv32_imem - neorv32_imem_   | 🕒 Open File          |                       | Alt+0       | 27-10 (xc72010clg400-1)   |                                     |  |        |
| IP Integrator                               | Constraints (1)  | Replace File         |                       |             | v32_test_setup_bootloade  | 1                                   |  | - 1    |
| 👬 Create Block Design                       |  | Copy File Into Pr    | oject                 |             |   |                                     |  |        |
| 😚 Open Block Design                         |  | Copy All Files Int   | o Project             | Alt+I       | 2   |                                     |  | _      |
| 🍪 Generate Block Design                     |  | Enable File          | n Project             | Delete      |   |                                     |  |        |
| Simulation                                  | Hierarchy IP Sources Libraries Com   | Disable File         |                       | Alt+Minus   | 7-10  |                                     |  |        |
| Simulation Cettings                         | Source File Properties Move to Simulation  |                      | ion Sources           |             | inc.com:zybo-z7-10:part0:1  | .1                                  |  |        |
| Bun Simulation                              | ← → 10 k   | Move to Design       | Sources               |             | nx/Vivado/2016.4/data/boa   | rds/board_files                     |  |        |
|   | riscv_wrapper_wrapper.vhd  | Hierarchy Updat      | e                     | •           | <ul> <li>digilent.com/reference/programmable-logic/zybo-z7/start</li> </ul> |                                     |  |        |
| RTL Analysis                                | C Enchlad  | Refresh Hierard      | ny                    |             | 7-10  |                                     |  |        |
| 6 Elaboration Settings                      | erabled  | IP Hierarchy         |                       | •           |   | Implementation                      | n  |        |
| Open Elaborated Design                      | Location: /nome/tretz/wsp/vivado   | Set Global Inclu     | de la                 |             |   | Status                              | and the set stress   |        |
| Synthesis                                   | Type: VHDL -   | Clear Global Incl    | ude                   |             |   | Status:                             | Cut-on-date  |        |
| Synthesis Settings                          | Library: neory32 -   | Set as Out-of-Co     | intext for Synthesis. |             | 1.1   | Port.                               | 1 84 warnings  |        |
| Run Synthesis                               | General Properties   | Set Library          |                       | Alt+L       | sis Defaults  | Strategy                            | Weado Implementation Defaults                                  | 5      |
| Open Synthesized Design                     |  | Set File Type        |                       |             |   | birdiogy.                           | wado implementation perauto                                    |        |
|   | Tci Console  | Set Used In          |                       |             |   |                                     | ? = 🗆 1  |        |
| Implementation                              | reset_target all [get_files  | Edit Constraints     | Sets                  |             | rcs/sources_1/bd/riscv_v  | vrapper/riscv_wrapper.bd            | 1]   |        |
| Implementation Settings                     | export_ip_user_files -of_obje  | Edit Simulation :    | sets                  |             | neorv32/neorv32.srcs/sou  | <pre>inces_1/bd/riscv_wrapper</pre> | <pre>/riscv_wrapper.bd] -sync -no_script -force bdl -top</pre> | -9     |
| Fun implementation                          | Adding cell xilinx.com:ip:   | Add Sources          |                       | AETA        | .a.ca/addrees_1/0d/F15C   | Tereshers, raceTerabber.            | and con  |        |
| <ul> <li>Open implemented Design</li> </ul> | WHDL Output written to : /hom  | - Report in Status   | noincts (nenry 22 /ne | arv22 erre  | sources_1/bd/riscv_wrapp  | er/hdl/riscv_wrapper.vh             | id   |        |
| Program and Debug                           | Wrote : <td>ado_projects/neorv3</td> <td>2/neorv32.srcs/sour</td> <td>rces_1/bd/r</td> <td>iscv_wrapper/riscv_wrappe</td> <td>er.bd&gt;</td> <td>apper . ma</td> <td></td> | ado_projects/neorv3  | 2/neorv32.srcs/sour   | rces_1/bd/r | iscv_wrapper/riscv_wrappe   | er.bd>                              | apper . ma   |        |
| 🚯 Bitstream Settings                        | add_files -norecurse /home/fro   | etz/wsp/vivado_proje | ects/neorv32/neorv3   | 32.srcs/sou | rces_1/bd/riscv_wrapper/h   | ndl/riscv_wrapper_wrappe            | en, vhd  |        |
| 🐏 Generate Bitstream                        |  |                      |                       |             |   |                                     |  | _      |
| Open Hardware Manager                       | Tune a Tel compand have  |                      | 1000                  |             |   |                                     |  |        |
|   | Tel Consolo O Massagas Filia   | a Banarte B D        | sign Runs             |             |   |                                     |  |        |
|   | a rei console Messages La Lo   | g 🗌 📾 neports 🗋 🧈 De | sign runs             |             |   |                                     |  |        |
| iet as Top                                  |  |                      |                       |             |   |                                     |  |        |

• Open the XDC file of the board to connect the NEORV32 ports to the appropriate pins of the FPGA.



· You should modify the following pins

| 1 | ## RISC-V Reset                                 |  |
|---|---|--|
| 2 | <pre>set_property -dict { PACKAGE_PIN K18</pre> | <pre>IOSTANDARD LVCMOS33 } [get_ports { ADD_PORT }]; #IO_L12N_T1_MRCC_35 Sch</pre> |
| 3 | # RISC-V LEDs                                   |  |
| 4 | <pre>set_property -dict { PACKAGE_PIN M14</pre> | <pre>IOSTANDARD LVCMOS33 } [get_ports { ADD_PORT }]; #I0_L23P_T3_35 Sch=led[</pre> |
| 5 | ##Pmod Header JC                                |  |
| 6 | <pre>set_property -dict { PACKAGE_PIN V15</pre> | <pre>IOSTANDARD LVCMOS33 } [get_ports { ADD_PORT }]; #IO_L10P_T1_34 Sch=JC1_</pre> |
| 7 | <pre>set_property -dict { PACKAGE_PIN W15</pre> | <pre>IOSTANDARD LVCMOS33 } [get_ports { ADD_PORT}]; #IO_L10N_T1_34 Sch=JC1_N</pre> |

• Save the XDC file and press the Generate Bitstream button. This will generate the bitstream after synthesis and implementation are successfully finished.

|  | neorv32 - [/home/fretz/wsp/vivado_   | projects/neorv32/neorv32.xpr] - Vivado 2016  | .4   |   |
|--|--|--|--|---|
| jle <u>E</u> dit Flow <u>T</u> ools <u>W</u> indow La  | wout View Help   |  |  | Q+ Quick Access                                   |
| 👌 🕼 🖓 🐚 🐘 🗙 🔌 🎽 🤅  | 🗟 🐝 🔽 🧔 🖾 Default Layout 🛛 🔹 🗶 🐁   |  |  | Re  |
| low Navigator ? «  | Project Manager - neorv32  |  |  | ?   |
| 入 🎞 🕸  | Sources ? = □ L <sup>8</sup> ×   | E Project Summary X  |  | ? 🗆 Ž ×   |
| Project Manager  | <ul> <li>3 (1) (1) (1) (1) (1) (1) (1) (1) (1) (1)</li></ul>   | Project Settings   |  | Edit  |
| Project Settings   | Messages: () <u>4 warnings</u>   | Project settings   |  | h.M.X.  |
| Add Sources     Language Templates     IP Catalog     IP Integrator     Accorate Block Design  | Uesign sources (a) I esign sources (a)   | Project location: /home/fretz/wspi/ivado<br>Product family: Zynq-7000<br>Project part: Zyho Z7-30 (xc7z0) 0/c/<br>Top module name: neon/32 test setup bo<br>Target language: VHDI  | projects/neorv32<br>1400-1)<br>otloader  |   |
| Copen Black Design   | ∳→ constraints (1)   | Simulator language: Mixed  |  |   |
| \delta Generate Black Design   | Zybo-Z7-Master.xdc     Simulation Sources (4)  | Board Part   |  |   |
| Simulation<br>Simulation Settings<br>Run Simulation  | •  | Display name: Zybo 27-10<br>Board part name: digilentinc.com:zybo-z7-10<br>Repository path: /opt/Xilinv/Vivado/2016.4/d<br>URL: https://digilent.com/refere  | :part0:1.1<br>lata/boards/board_files<br>.nce/programmable-logic/zy  | bo-27/start                                       |
| RTL Analysis   | Hierarchy IP Sources Libraries Compile Order   | Board overview: Zybo Z7-10   |  |   |
| <ul> <li>Baboration Settings</li> <li>B Open Elaborated Design</li> </ul>  | Source File Properties ? - C 2 ×   | Synthesis  | Implementation   |   |
| Synthesis  | 2ybo-Z7-Master.xdc   | Status: Not started  | Status:  | Not started                                       |
| <ul> <li>Synthesis Settings</li> <li>Run Synthesis</li> </ul>  | General Properties   | Part: xc7z010clg400-1<br>Strategy: Vivado Synthesis Defaults   | Part:<br>Strategy:   | xc7z010cig400-1<br>Vivado Implementation Defaults |
| Open Synthesized Design  | Tcl Console  |  |  | ? - 🗆 🖻   |
| Implementation Implementation Settings Run Implementation Run Implementation Implemented Design Program and Debug Bitstream Settings | <ul> <li>WOL Output vritten to : /nose/freiz/xsp/vixed_projects/nee</li> <li>WOL Output vritten to : /nose/freiz/xsp/vixed_projects/neorv32</li> <li>Wote : </li> <li>Abber/freiz/xsp/vixed_projects/neorv32</li> <li>add_files -norceurse /nose/freiz/xsp/vixed_projects/neorv32</li> <li>Bake_vrapper - files [get_files /hose/freiz/xsp/vixed_projects/neorv32</li> <li>Abber/files -norceurse /nose/freiz/xsp/vixed_projects/neorv32</li> <li>Bake_vrapper - files [get_files /hose/freiz/xsp/vixed_projects/neorv32</li> <li>Abber/files -norceurse /nose/freiz/xsp/vixed_projects/neorv32</li> <li>Abber/files -norceurse /nose/freiz/xsp/vixed_projects/neorv32</li> <li>Abber/files -norceurse /nose/freiz/xsp/vixed_projects/neorv32</li> <li>Abber/files -norceurse /nose/freiz/xsp/vixed_projects/neorv32</li> </ul>  | <pre>vr32/heorv32 srcs/sources 1/bd/riscv_vrapper/<br/>rv32/heorv32 srcs/sources 1/bd/riscv_vrapper/<br/>scs/sources 1/bd/riscv_vrapper/hd/v<br/>/heorv32 srcs/sources 1/bd/riscv_vrapper/hd/v<br/>ts/heorv32 srcs/sources 1/bd/riscv_vrapper/<br/>validated. Therefore parameter propagation vi<br/>vr32/heorv32 srcs/sources 1/bd/riscv_vrapper/<br/>rv32/heorv32 srcs/sources 1/bd/riscv_vrapper/<br/>rv32/heorv32 srcs/sources 1/bd/riscv_vrapper/</pre> | hdl/riscv_wrapper.vhd<br>hdl/riscv_wrapper_wrappe<br>ds<br>riscv_wrapper_wrapper.vh<br>apper/riscv_wrapper.bd]<br>ll not be re-run.<br>hdl/riscv_wrapper.vhd<br>hdl/riscv_wrapper_wrappe | ir.vhd<br>id<br>-top<br>ir.vhd                    |
| Open Hardware Manager  | <ul> <li>Image: A second s</li></ul> |  |  | 4   |
| -  | Type a Tcl command here  |  |  |   |
|  | 🗏 Tcl Console 🔎 Messages 🔍 Log 🏠 Reports 🕸 Design Runs   |  |  |   |
| enerate a programming file after imp   | plementation   |  |  |   |

• When the bitstream generation finishes, open to see the implemented design



# Board setup and run hello world software on the NEORV-32

• In order to get UART access on NEORV-32, we need to connect a USB/TTL UART external board on the PMOD header JC.

|      |     | _ | Data | pins |   |
|------|-----|---|------|------|---|
| 3.3V | GND | 3 | 2    | 1    | 0 |
| 3.3V | GND | 7 | 6    | 5    | 4 |



- Now, Programm the FPGA
- Once you program the FPGA you should see that the LD0 blinks (left side of the photo) after you press the reset button (right side of the photo). Also, the PGOOD and DONE leds should be ON.



- Open a terminal and press cutecom
- Click on settings and configure as follows and then click on open

| Activitie | 🖾 CuteCom 🕶   | Feb 9 09:32          |                         |                     | A 🛭 O 🗕 |
|-----------|---|----------------------|-------------------------|---------------------|---------|
| (         |   |                      |                         |                     |         |
|           | Fretz@ubuntu: -   |                      |                         | stz@ubuntu: ~       |         |
|           | fretz@ubuntu:~\$ cutecom  |                      |                         |                     |         |
| ×         | setting current session to: "Default"   |                      |                         |                     |         |
|           | MainWindow::MainWindow(QWidget*, const  | QString&)            | calculated              | height: 31          |         |
| •         | fretz@ubuntu:~\$ Cutocom  | CuteCom - Default    |                         | - • 🙁               |         |
| . /       | SETTING CURRENT SE Sessions Help<br>Baudrate 19200 * Data Bits 8 * Display Ct | rl characters        |                         |                     |         |
|           | MainWindow::MainWi Flow Control None - Parity None - Show Time                | estamp               |                         | -                   |         |
| 1         | Tretz@ubuntu:~\$ CU OpenMode Read/Write * Stop Bits 1 * Logfile: /hon         | me/fretz/cutecom.log | Append                  |                     |         |
| SDK       |   |                      |                         |                     |         |
|           | mainwindow::mainwin   |                      |                         |                     |         |
|           | sotting current co  |                      | None   Char delay: 0 ms | Send file     Plain |         |
|           | Setting Current Set   |                      |                         |                     |         |
| N         |   |                      |                         |                     |         |
|           |   |                      |                         |                     |         |
|           |   |                      |                         |                     |         |
|           |   |                      |                         |                     |         |
|           |   |                      |                         |                     |         |
|           |   |                      |                         |                     |         |
|           |   |                      |                         |                     |         |
|           | Clear Hex output Logging to: /home/fretz/cutecon                              | m.log                |                         |                     |         |
|           | Device: /dev/ttyUS80 Connection: 19200 @ 8-N-1                                |                      |                         |                     |         |
|           |   |                      |                         |                     |         |
|           |   |                      |                         |                     |         |
|           |   |                      |                         |                     |         |

Select None

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|-----------|---|--------------------------------|--|---------|
| 6         |   |                                |  | Q =     |
| _         |   |                                |  | × +     |
| •         | <pre>fretz@ubuntu:~\$ cutecom</pre>   |                                |  |         |
| ×         | setting current session to: "Def  | fault"                         |  |         |
|           | MainWindow::MainWindow(QWidget*,  | <pre>const QString&amp;)</pre> | calculated height: 31                      |         |
| • ^-      | <pre>fretz@ubuntu:~\$ cutocom</pre>   | CuteCom - Default              | - • 🙁                                      |         |
|           | setting current se Sessions Help  |                                | Satting                                    |         |
| · 🖉       | MainWindow::MainWil   |                                | - Second                                   |         |
|           | fretz@ubuntu:~\$ cu   |                                |  |         |
|           | setting current se  |                                | LF.  |         |
| SDK       | MainWindow::MainWil   |                                | CR .                                       |         |
|           | fretz@ubuntu:~\$ cu:  |                                | CR/LF Char delay: 0 ms + Send file Plain + |         |
|           | setting current se  |                                | Hex  |         |
|           | MainWindow::MainWi  |                                |  |         |
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|           |   |                                |  |         |
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|           |   |                                |  |         |
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|           |   |                                |  |         |
| /         |   |                                |  |         |
|           | Clear Hex output Logging to: /<br>Device: 1a86 USB2.0-Ser @ttvUSB0 Connection | nome/fretz/cutecom.log         |  |         |
|           |   |                                |  |         |
| /         |   |                                |  |         |
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• In the input, add the character a, press the reset button of NEORV32-V on the board and then press enter on cutecom

| Activities 🖾 CuteCom 🕶          |  | Feb 9 09:36       |  |          | ▲ ● ७ ◄ |
|---------------------------------|--|-------------------|--|----------|---------|
| 🐴 🖪                             |  |                   |  |          |         |
| tre                             |  |                   |  |          |         |
| · fretz@ubuntu:~\$ cut          | tecom  |                   |  |          |         |
| setting current ses             | sion to: "Defau  | lt"               |  |          |         |
| MainWindow::MainWir             | ndow(OWidget*. co  | nst OString&)     | calculated hei                           | aht: 31  |         |
| <pre>fretz@ubuntu:~\$ cu*</pre> |  | ,                 |  |          |         |
| <pre>setting current se</pre>   | Sessions Help  | CuteCom - Default |  | - • •    |         |
| MainWindow::MainWi              | Close Device: /dev/ttyUSB0 *   |                   |  | Settings |         |
| ↓ fretz@ubuntu:~\$ cu           | j  |                   |  |          |         |
| setting current se              | ;mm';m';   |                   |  |          |         |
| SOK MainWindow · · MainWi       | k  |                   |  |          |         |
| □ fretz@ubuntu:~\$ cu           | a  |                   |  |          |         |
| Setting current se              | Input: a 1   |                   | None * Char delay: 0 ms Char delay: 0 ms | d file   |         |
| MainWindow··MainWi              | HWV: 0x01080000<br>CID: 0x00000000                                       |                   |  |          |         |
|                                 | CLK: 0x05f5e100<br>ISA: 0x40801104 + 0x00000081                          |                   |  |          |         |
|                                 | IMEM: 0x00004000 bytes @0x00000000<br>DMEM: 0x00002000 bytes @0x80000000 |                   |  |          |         |
|                                 | Autoboot in 8s. Press any key to abort.                                  |                   |  |          |         |
|                                 | Available CMDs:  |                   |  |          |         |
|                                 | h: Help<br>r: Restart  |                   |  |          |         |
|                                 | s: Store to flash<br>L Load from flash                                   |                   |  |          |         |
|                                 | x: Boot from flash (XIP)<br>e: Execute                                   |                   |  |          |         |
|                                 | CMD:>  | etz/cutecom.log   |  |          |         |
|                                 | Device: /dev/ttyUSB0 Connection: 19200 @ 8-N-1                           |                   |  |          |         |
|                                 |  |                   |  |          |         |
|                                 |  |                   |  |          |         |
|                                 |  |                   |  |          |         |
|                                 |  |                   |  |          |         |

## Setup RISC-V compiler

Skip these steps if you have the Fretz virtual machine.

- Open the Fretz VM and install  $\ensuremath{\mathsf{cutecom}}$  , and the RISC-V compile flow
- In a terminal type, the following

```
1 $ sudo apt install cutecom -y
```

2 \$ cd ~/wsp/Downloads/

3 \$ wget https://github.com/stnolting/riscv-gcc-prebuilt/releases/download/rv32i-2.0.0/riscv32-unknown-elf.gcc-10.2

Create a folder where you want to install the toolchain, for example /opt/riscv (you will need sudo rights to create this folder and copy data to it).

1 \$ sudo mkdir /opt/riscv

Navigate to the download folder. Decompress your toolchain (replace TOOLCHAIN with your toolchain archive of choice). Again, you might have to use sudo if your target directory is protected.

1 \$ sudo tar xzfv riscv32-unknown-elf.gcc-10.2.0.rv32i.ilp32.newlib.tar.gz -C /opt/riscv/

Now add the toolchain's bin folder to your system's PATH environment variable (or add this line to your .bashrc if applicable):

1 \$ export PATH=\$PATH:/opt/riscv/bin

Test the toolchain:

```
1 $ riscv32-unknown-elf-gcc -v
```

### Continue from here: Compile your first hello world example!!!!

· Let's download some application examples. Open a terminal and type

```
1 cd ~/wsp/neorv32/sw/example/hello_world
```

- 2 make clean\_all
- 3 make
- On cutecome enter the character u and press enter
- 1 CMD:> u
  2 Awaiting neorv32\_exe.bin...
- On cutecome click the send file button

| Activitie | es 🖾 CuteCom 🔻                 | Feb 9 09:38  | A 🛭 🖱 🗸   |
|-----------|--------------------------------|--|---|
| (         |                                |  |   |
|           |                                |  | fretz@ubuntu: -/wsp/neorv32/sw/example × -            |
| •         | make[1]: Leaving di            | rectory '/home/fretz/wsp/neorv32/sw/exa  | <pre>mple/demo_freeRTOS'</pre>                        |
| ×         | <pre>make[1]: Entering d</pre> | irectory '/home/fretz/wsp/neorv32/sw/ex  | ample/demo_gptmr'                                     |
|           | /opt/riscv/bin//l              | .ib/gcc/riscv32-unknown-elf/10.2.0//   | ///riscv32-unknown-el                                 |
| • *-      | f/bin/ld: warning:             | connect find ontail or the deferring current of the deferring current o | +i~~_t~_ <u>_</u>                                     |
|           | Memory utilization             | Sgssions Help  |   |
| • 🖊       | text data                      | Close Device: //dev/ttyUS80 7  | Settings  |
|           | 3488 0                         | j<br>h   |   |
|           | Executable (neorv3)            | "mm";m";<br>Im   |   |
| SDK       | 3500                           |  |   |
|           | Installing applica             | Inout: a None Y Char delay:  | ams : send file, Plain , mage.vhd                     |
| لكا       | <pre>make[1]: Leaving d</pre>  | BLDV: Jan 21 2023  | Select a file to be sent using the specified protocol |
|           | make[1]: Entering              | HWV: 0x01080000<br>(D): 0x00000000<br>(D): 0x0000000   | rigger module   |
|           | ·                              | ISA: 0x4000104 + 0x0000081<br>SC: 0x0007000d   |   |
|           | /ont/riscy/hin/ /              | IMEM: 0x00004000 bytes @0x00000000<br>DMEM: 0x00002000 bytes @0x80000000   | 2-unknown-el  |
|           | f/bin/ld: warning:             | Autoboot in 8s. Press any key to abort.<br>Aborted   |   |
|           | Memory utilization             | Available CMDs:  |   |
|           |                                | h: Help<br>r: Restart  |   |
|           |                                | s: Store to flash<br>1: Load from flash  |   |
|           | 4396 0                         | x: Boot from flash (XIP)<br>e: Execute   |   |
|           | Executable (neorv3             | CMD:>  | w.  |
| - 7       | 4408                           | Clear Hex output Logging to: /nome/tretz/cutecom.log   |   |
|           | Installing applica             | ion image to///rtl/core/neorv32_   | _application_image.vhd                                |
|           | <pre>make[1]: Leaving di</pre> | rectory '/home/fretz/wsp/neorv32/sw/exa  | mple/demo_trigger_module'                             |
|           | fretz@ubuntu:~/wsp/            | neorv32/sw/example\$   |   |

- If everything goes fine, OK will appear in your terminal:
- 1 CMD:> u
- 2 Awaiting neorv32\_exe.bin... OK
- The executable is now in the instruction memory of the processor. To execute the program right now, run the "Execute" command by

typing e in cutecome and press the Enter on your keyboard:

| CuteCom - Default  |  |             |       |           |       | <b>- 8</b> |
|--|--|-------------|-------|-----------|-------|------------|
| Sessions Help  |  |             |       |           |       |            |
| Close Device: /dev/ttyUSB0 >   |  |             |       |           |       |            |
| h  |  |             |       |           |       | -          |
| n<br>n<br>n<br>n   |  |             |       |           |       |            |
| im in i  |  |             |       |           |       |            |
| k  |  |             |       |           |       |            |
|  |  |             |       |           |       |            |
| a  |  |             |       |           |       |            |
| e  |  |             |       |           |       |            |
|  |  |             |       | 10        | 10    | *          |
| Input:   | None *   | Char delay: | 0 ms  | Send file | Plain | *          |
| s: Store to flash<br>1: Load from flash<br>2: Door from flash<br>2: Door from flash (XP)<br>CMOD: =<br>Booting from 0x00000000 | # ## ##<br>####<br>###<br>\$###<br>################# | *****       | ***** |           |       | ×          |
| Device: /dev/ttyUSB0 Connection: 19200 @ 8-N-1   |  |             |       |           |       |            |

- Read 
   [User Guide] The NEORV32 RISC-V Processor section 6
- 6. Installing an Executable Directly Into Memory

If you do not want to use the bootloader (or the on-chip debugger) for executable upload or if your setup does not provide a serial interface for that, you can also directly install an application into embedded memory.

This concept uses the "Direct Boot" scenario that implements the processor-internal IMEM as ROM, which is pre-initialized with the application's executable during synthesis. Hence, it provides *non-volatile* storage of the executable inside the processor. This storage cannot be altered during runtime and any source code modification of the application requires to re-program the FPGA via the bitstream.

See datasheet section Direct Boot for more information.

Using the IMEM as ROM:

- · for this boot concept the bootloader is no longer required
- this concept only works for the internal IMEM (but can be extended to work with external memories coupled via the processor's bus interface)
- make sure that the memory components (like block RAM) the IMEM is mapped to support an initialization via the bitstream
- 1. At first, make sure your processor setup actually implements the internal IMEM: the MEM\_INT\_IMEM\_EN generics has to be set to true:

Listing 8. Processor top entity configuration - enable internal IMEM

- 1 -- Internal Instruction memory --
- 2 MEM\_INT\_IMEM\_EN => true, -- implement processor-internal instruction memory
- 2. For this setup we do not want the bootloader to be implemented at all. Disable implementation of the bootloader by setting the INT\_BOOTLOADER\_EN generic to false. This will also modify the processor-internal IMEM so it is initialized with the executable during synthesis.

Listing 9. Processor top entity configuration - disable internal bootloader

```
1 -- General --
2 INT_BOOTLOADER_EN => false, -- boot configuration: false = boot from int/ext (I)MEM
```

3. To generate an "initialization image" for the IMEM that contains the actual application, run the install target when compiling your application:

| 1 | <pre>neorv32/sw/example/demo_blink_led\$ make clean_all install</pre> |         |           |          |     |            |           |          |          |        |
|---|---|---------|-----------|----------|-----|------------|-----------|----------|----------|--------|
| 2 | Memory utilization:   |         |           |          |     |            |           |          |          |        |
| 3 | text  | data    | bss       | dec      | hex | filename   |           |          |          |        |
| 4 | 1004  | Θ       | Θ         | 1004     | 3ec | main.elf   |           |          |          |        |
| 5 | Compiling//sw/image_gen/image_gen                                     |         |           |          |     |            |           |          |          |        |
| 6 | Executable (neorv32_exe.bin) size in bytes:                           |         |           |          |     |            |           |          |          |        |
| 7 | 1016  |         |           |          |     |            |           |          |          |        |
| 8 | Installing  | applica | ation ima | age to . | .// | /rtl/core/ | /neorv32_ | applicat | ion_imag | ge.vhd |
|   |   |         |           |          |     |            |           |          |          |        |

- 4. The install target has compiled all the application sources but instead of creating an executable (neorv32\_exe.bit) that can be uploaded via the bootloader, it has created a VHDL memory initialization image core/neorv32\_application\_image.vhd.
- 5. This VHDL file is automatically copied to the core's rtl folder (rtl/core) so it will be included for the next synthesis.
- 6. Perform a new synthesis. The IMEM will be build as pre-initialized ROM (inferring embedded memories if possible).
- 7. Upload your bitstream. Your application code now resides unchangeable in the processor's IMEM and is directly executed after reset.

The synthesis tool / simulator will print asserts to inform about the (IMEM) memory / boot configuration:

- 1 NEORV32 PROCESSOR CONFIG NOTE: Boot configuration: Direct boot from memory (processor-internal IMEM).
- 2 NEORV32 PROCESSOR CONFIG NOTE: Implementing processor-internal IMEM as ROM (1016 bytes), pre-initialized with app