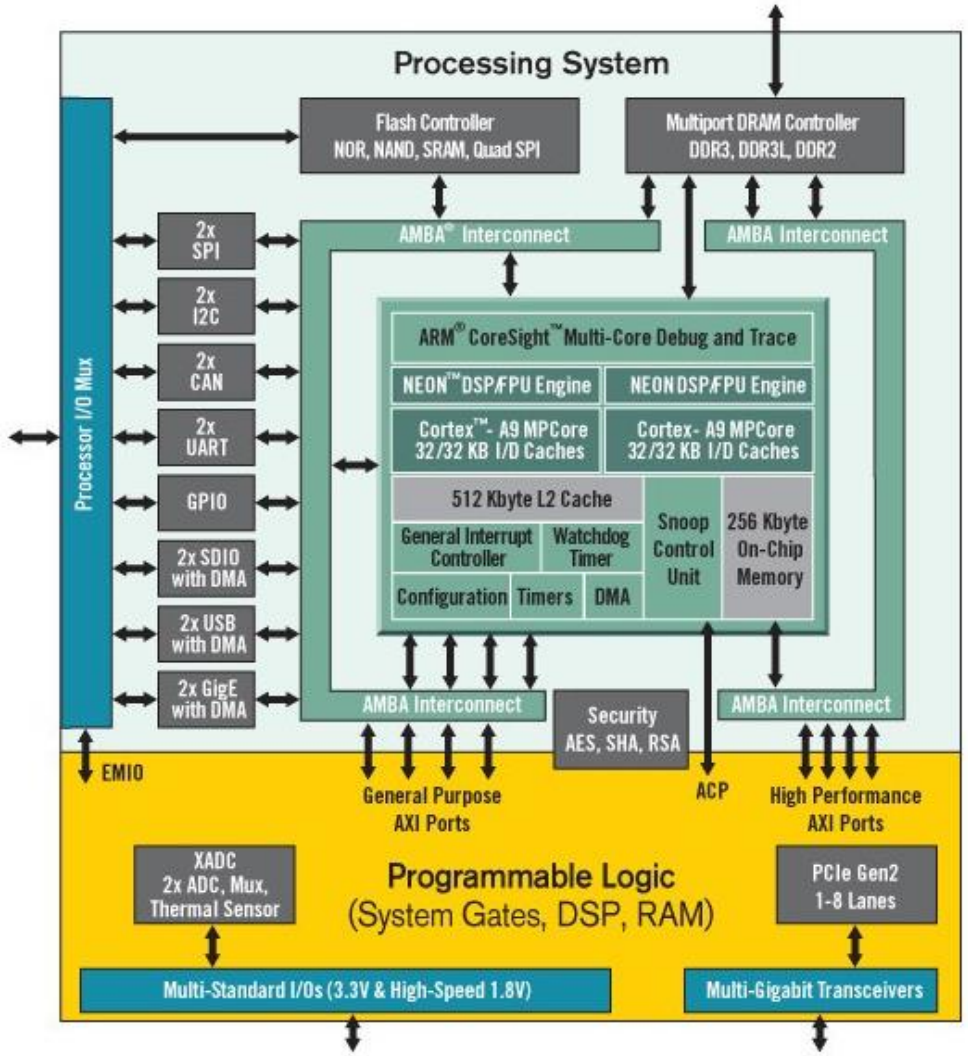
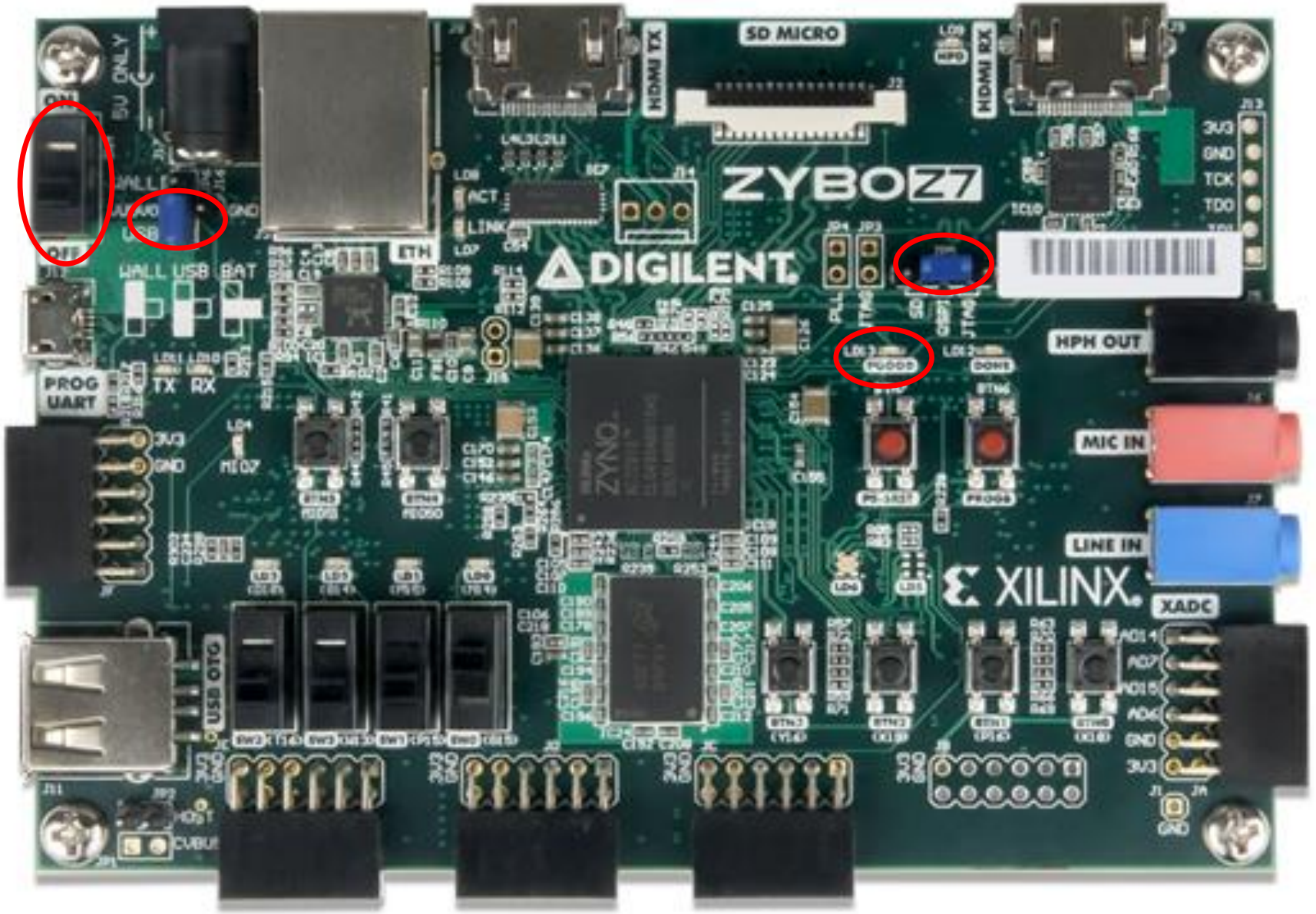
Zybo Z7-10 Lab Design Flow Overview

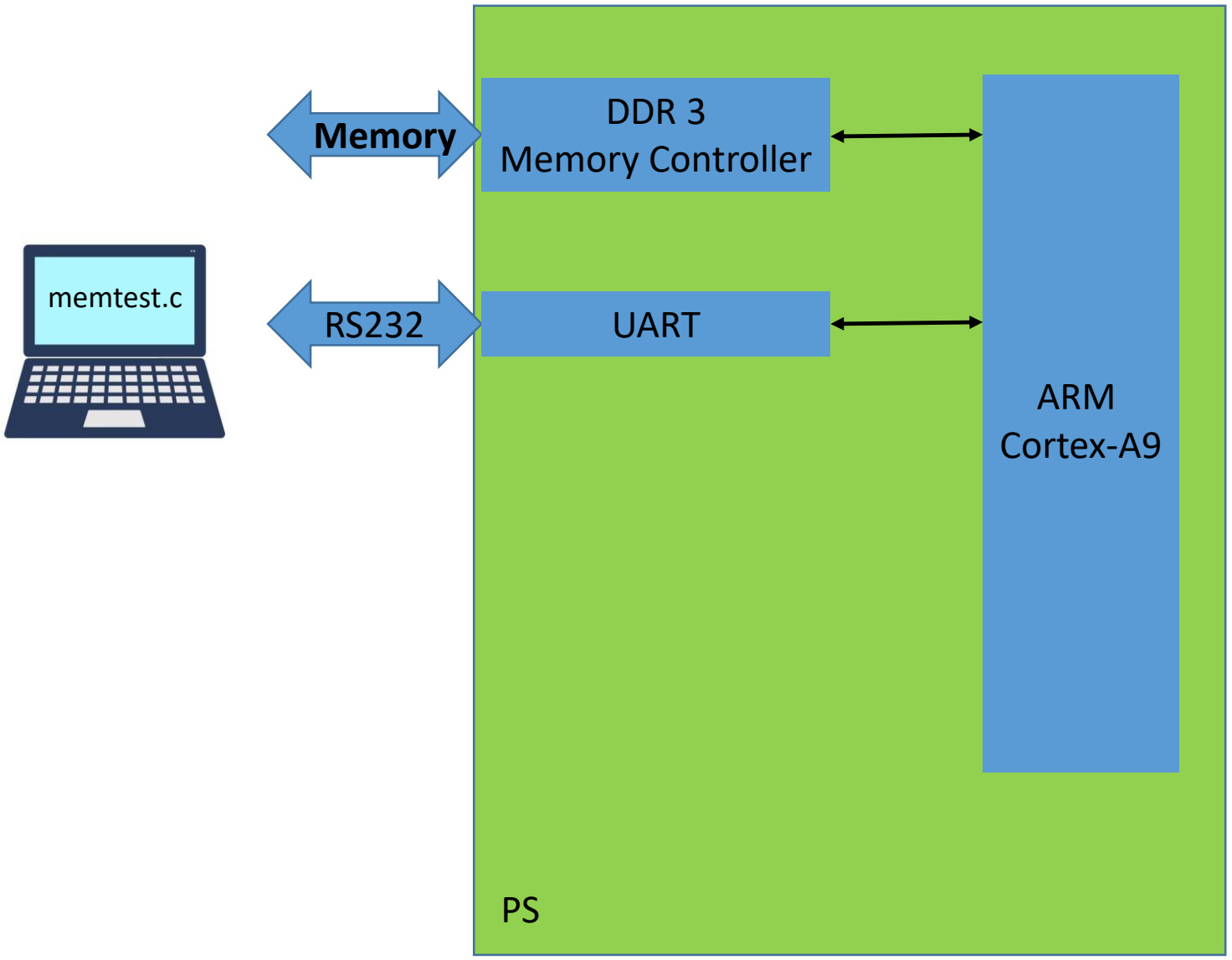
Xilinx Processing System and Programmable Logic Chip



Zybo Z7-10 Board



Zybo Lab 1 Design Flow Overview



Zybo Lab 1 Design Flow Overview

Create Project (Vivado)

File->Project->New

board: **Zybo Z7-10**

Create PS (Vivado)

Create Block Design

name: system

Add IP

ZYNQ7 P.S.

Run Block Automation

Re-customize IP

UART1 only

MIO Configuration->I/O Peripherals->
Deselect **ENET0,USB0,SD0,GPIO MIO**
MIO Configuration->Memory Interfaces>
Deselect **QUAD SPI Flash**
MIO Configuration->Application Processor Unit>
Deselect **Timer0**

PS-PL Configuration->AXI Non Secure->…->
Deselect **M AXI GP0**
PS-PL Configuration-> General>Enable Clock Resets->
Deselect **FCLOCK_RESET0_N**
Clock Configuration-> PL Fabric Clocks->
Deselect **FCLOCK_CLK0**

Validate Design

Generate Top Level HDL And Export to SDK (Vivado)

Generate Block Design

Create HDL Wrapper

.bd file right click

Export Hardware

File->Export->Export Hardware (no bitstream)

Create App (SDK)

Launch SDK

File->Launch SDK

Create Application

File->New->Application Project (Templates: Memory Tests)

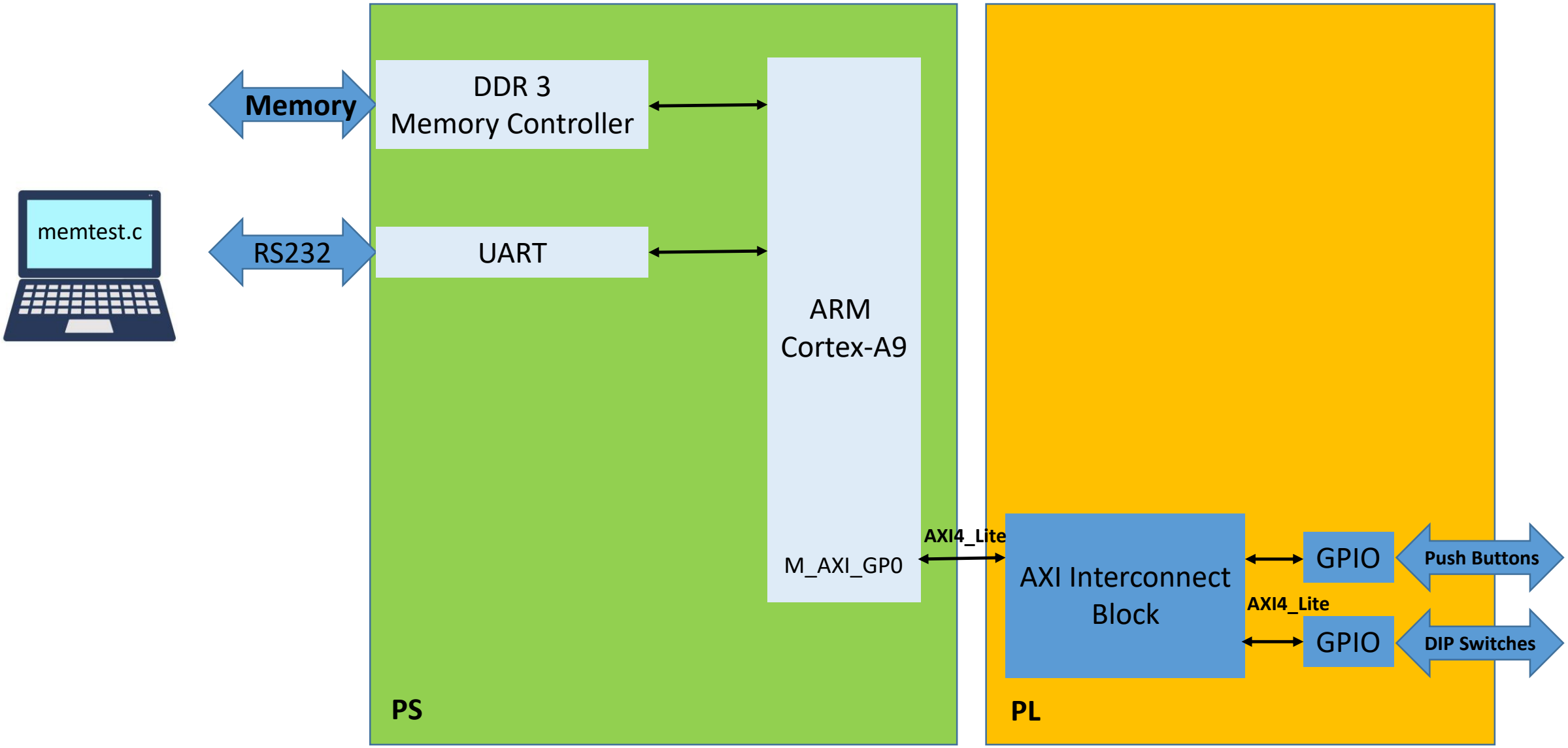
Verify in Hardware (SDK + Zybo)

Run As > Launch on Hardware (GDB)

Zybo: Select USB Power (JP7 or JP6)
Select JTAG Mode (JP5)
Connect USB cable + ON (SW4)

SDK: Window->Show View->Terminal
Settings: COMx,Serial,N81,115200

Zybo Lab 2 Design Flow Overview



Zybo Lab 2 Design Flow Overview (a)

Open and Save Project (Vivado)

File->Project->Open

lab1

File->Project->Save As

lab2

Add 2 GPIO (Vivado)

Open Block Design

Customize block

PS-PL Configuration->AXI Non Secure->…->
Select **M AXI GP0**
PS-PL Configuration-> General>Enable Clock Resets->
Select **FCLOCK_RESET0_N**
Clock Configuration-> PL Fabric Clocks->
Select **FCLOCK_CLK0 (100MHz)**

Add IP

AXI GPIO

Rename to: switches

Customize block

Led Width: **8**

Run Connection Automation

/switches/S_AXI

Add IP

AXI GPIO

Rename to: buttons

Customize block

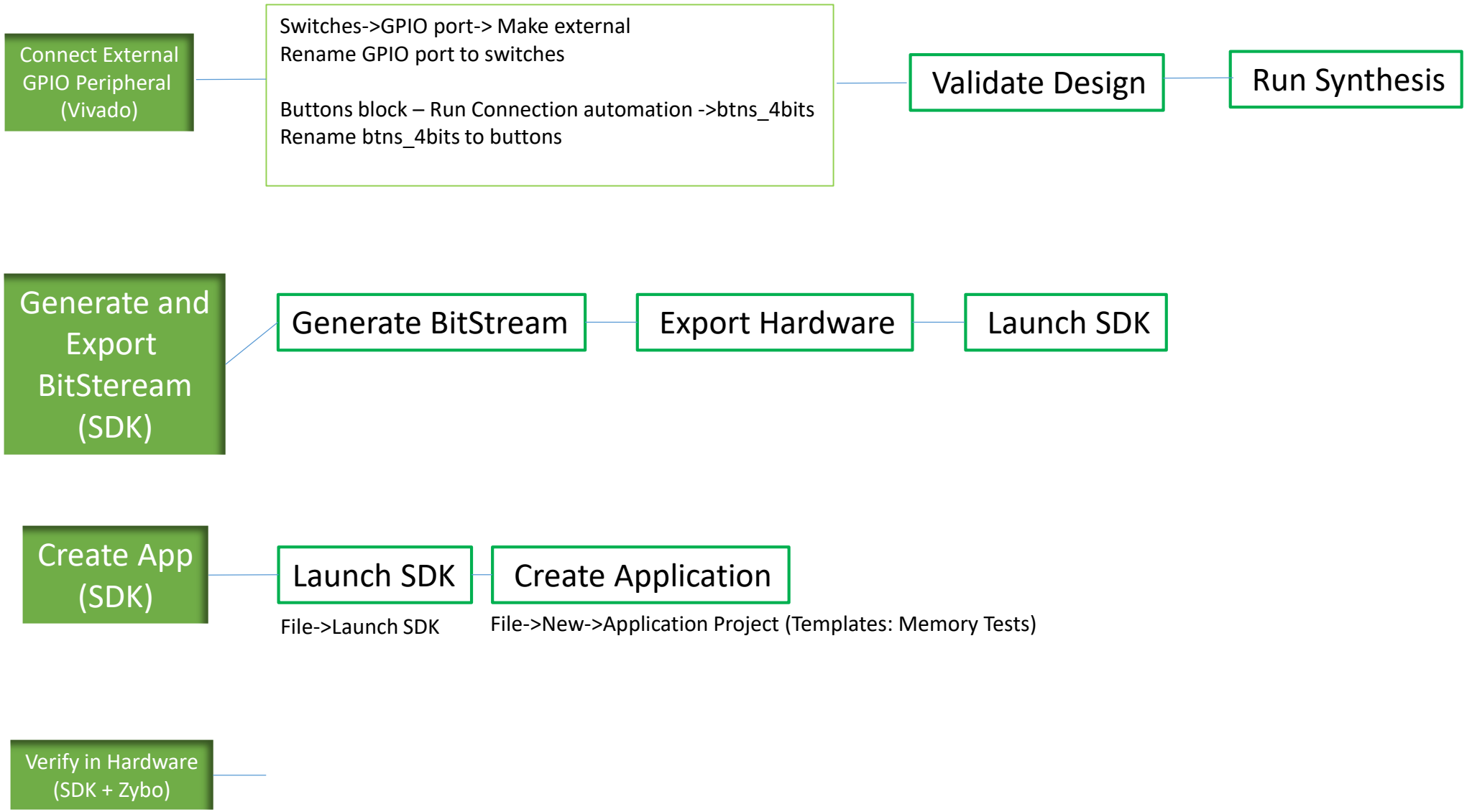
Board Interface: **btns 4bits**

Customize block

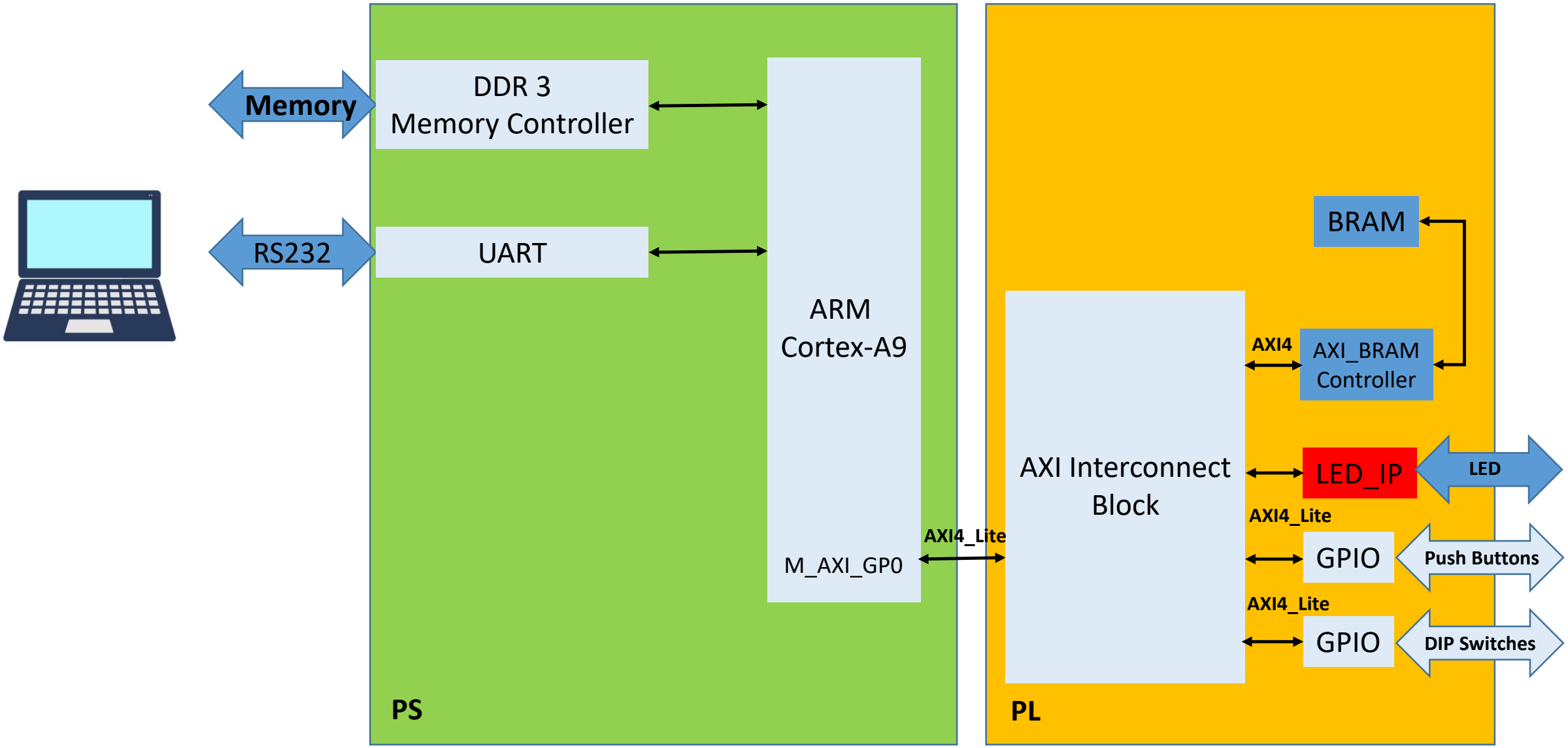
AXI Intercponnect:
Number of Master Interfaces**: 2**
Connect:
s_axi (buttons) -> AXI Interconnect
s_axi_aclk (buttons) -> Zynq7 Processing System FCLK_CLK0
s_axi_aresetn (buttons) -> Processor System Reset peripheral_aresetn
AXI Interconnect M01_ACLK -> Zynq7 Processing System FCLK_CLK0
AXI Interconnect M01_ARESETN -> Processor System Reset peripheral_aresetn

Address Editor:
Assign Addres

Zybo Lab 2 Design Flow Overview (b)



Zybo Lab 3 Design Flow Overview



Zybo Lab 3 Design Flow Overview (a)

Create Custom IP (Vivado)

File->IP->New Location

Part: Boards=**Zybo Z7-10**
Target Language: **Verilog**
Simulator Language: **Mixed**
Location: **…/projects/LED_IP**

Tools->Create and Package IP

Create **AXI4 Peripheral**
Name**: led_ip**
Add Interfaces**->**Name: **S_AXI**
Lite,Slave,32

Next Steps: **Edit IP**

Create Interface to LEDs

sources->led_ip_v1_0.v
Line 7: **parameter integer LED_WIDTH = 8,**
Line 18: **output wire [LED_WIDTH-1:0] LED,**
Line 48: **.LED_WIDTH(LED_WIDTH),**
Line 52: **.LED(LED),**

---

sources->…->led_ip_v1_0_S_AXI.v
Line 7: **parameter integer LED_WIDTH = 8,**
Line 18: **output wire [LED_WIDTH-1:0] LED,**
Line 400: Add user logic from file:
user_logic_instantiation.txt

Add Sources

Add or Create Design Sources
Add files: **lab3_user_logic.v**

Run Synthesis

Synthesis Completed:
Cancel

Package IP

Identification
Categories: from **AXI** to **Basic elements**
Combatibility: Family Zynq
File Groups: **Merge changes**
Custom. Param.: **Merge changes**
LED port -> Import param.
Review and Package: **Package**
Close Project

File->Close Project

Open and Save Project (Vivado)

File->Project->Open

lab2

File->Project->Save As

lab3

Zybo Lab 3 Design Flow Overview (b)

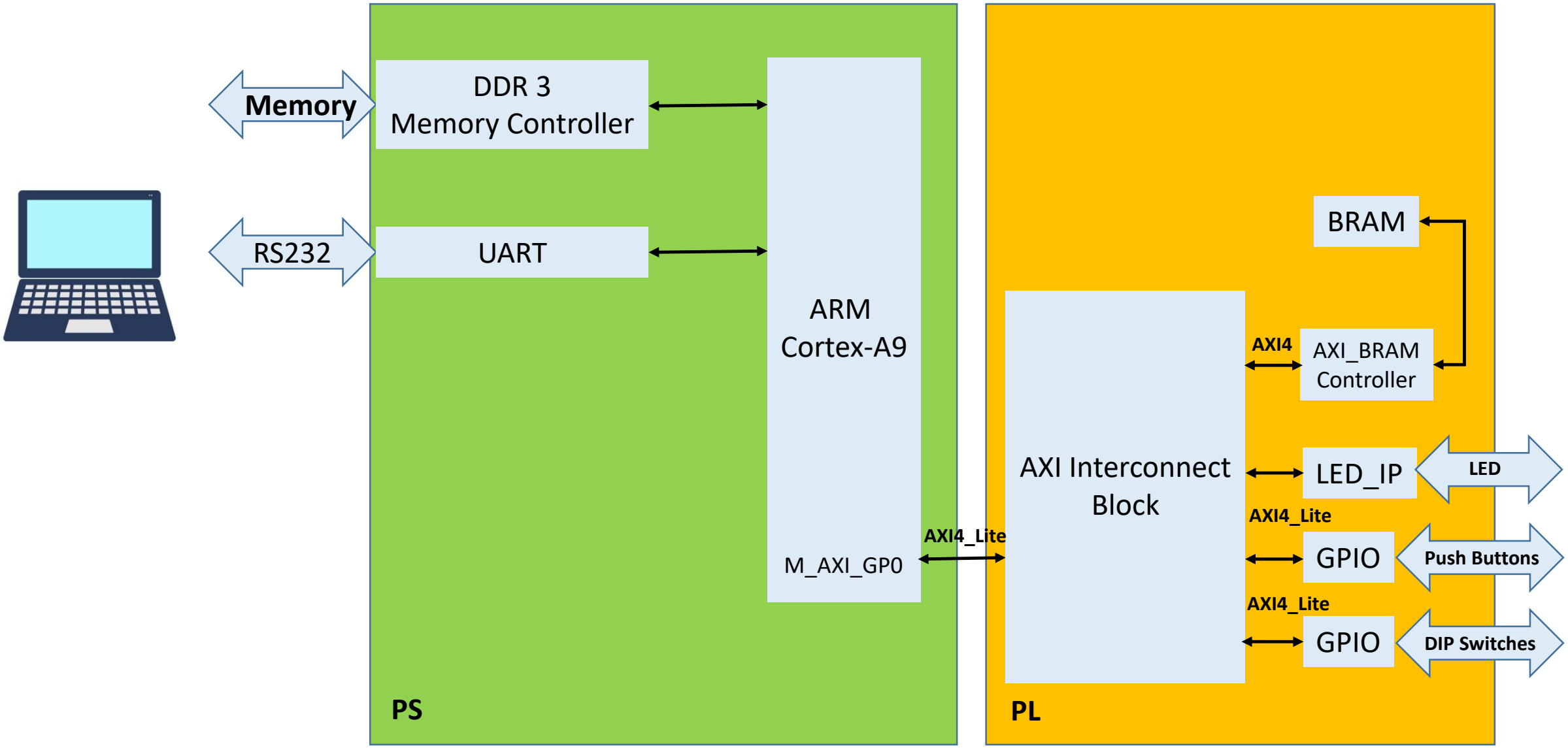
Set the Project Settings (Vivado)

- **Settings**
  - IP->Repository>ip_repo/led_ip_v1.0

Add LED,BRAM, Constraints (Vivado)

- **Open Block Design**
- **Add IP**
  - **led_ip_1.0**
  - Rename to: **led_ip**
- **Customize Block**
  - LED width: **4**
- **Run Connection Automation**
  - **led_ip/S_AXI**
- **Make External**
  - **LED[3:0]**
- **Add IP**
  - **AXI BRAM Controller**
- **Run Connection Automation**
  - **axi_bram_ctrl_0/S_AXI**
- **Customize Block**
  - Number of BRAM Interfaces:**1**
- **Run Connection Automation**
  - Generate Memory
- **Validate Design**
- **Add Sources**
  - Add or Create Design Constraints
  - Add files: **lab3_zybo.xdc**
- **Generate Output Products**
  - **System.bd**
- **Generate BitStream**

Zybo Lab 4 Design Flow Overview



Zybo Lab 4 Design Flow Overview (a)

Open and Save Project (Vivado)

File->Project->Open

lab3

File->Project->Save As

lab4

Create App (SDK)

Export Hardware

File->Export->Export Hardware
(include bitstream)

Launch SDK

File->Launch SDK

Create Application

Close Projects
File->New->Application Project: **lab4 - Empty**
lab4/src Import: **lab4.c**

Read Documentation

lab4_bsp/System.mss
Open xgpio.h

Edit lab4.c

Line 14: XGpio_Initialize(&dip, XPAR_SWITCHES_DEVICE_ID
Line 17: XGpio_Initialize(&push, XPAR_BUTTONS_DEVICE_ID);

lab4_bsp->Settings
View: projects\led__ip\ip_repo\led_ip_2.0\drivers\led_ip_v1_0\src

Line 3: #include "led_ip.h"
Line 29: LED_IP_mWriteReg(XPAR_LED_IP_S_AXI_BASEADDR, 0, dip_check);

Analyze Object (SDK)

Tools->Launch Shell

cd lab4\Debug
arm-xilinx-eabi-objdump –h lab4.elf

Verify in Hardware (SDK + Zybo)