AVR32111: Using the AVR32 PIO Controller

Features

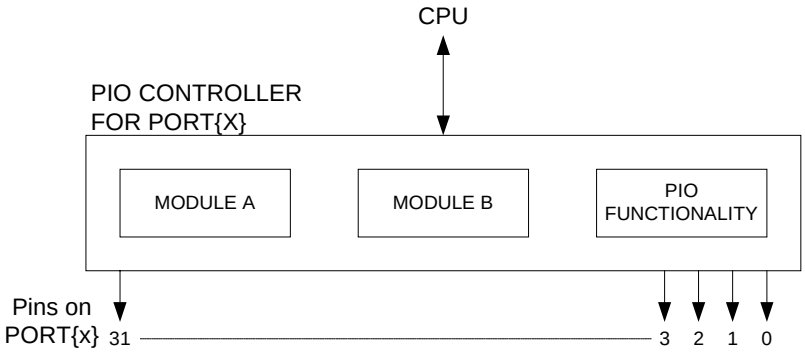
- **All I/O pins are configurable**
  - **PIO controllable**
  - **Module controllable**
- **Highly flexible**
  - **Set/Clear registers**
  - **Read status**
  - **Module operation**
  - **Level change Interrupt**
  - **Internal Pull-up**
  - **Glitch filter**
- **User configurable**

1 Introduction

The AVR®32 PIO Controller is responsible for selecting functionality on the I/O pins. This I/O can either be controlled by the PIO controller itself or by a module that is connected to the appropriate PIO. Up to two modules can be connected to a PIO for any given port.

Each port can be configured independently of each other and can be changed on the fly. The PIO controller has default settings according to the datasheet for any specific device, but the PIO controller has to be configured correctly for any module or general-purpose I/O operations can occur.

Figure 1.1: PIO Controller conceptual schematics



32-bit AVR® Microcontrollers

Application Note

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2 PIO Configuration

The PIO Controller is responsible for managing the I/O lines. It can either be in control itself or give the responsibility to another module connected to that specific PIO port. There can be up to two modules connected to the same I/O pin, and in addition to the PIO Controller. This ensures high I/O flexibility.

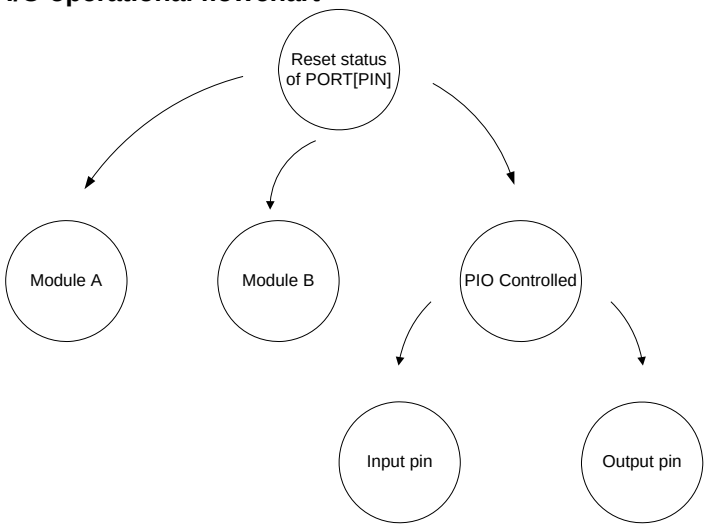
2.1 I/O Modules

All I/O operations go through the PIO Controller. There is an instance of the PIO Controller on each port of your device, and each port has up to 32 pins. The PIO Controller can either drive the pins itself or give the responsibility to one module out of possibly two connected modules.

- If it gives access to the pins to a module, the module is responsible for data and data direction. This is found in the module's specification and is not interfered by the PIO Controller.
- If the PIO Controller takes control over the pins itself, they can either be labeled as input or output.

The possible states for each pin are shown in Figure 2.1.

Figure 2.1: I/O operational flowchart



As the configuration can be set individually for each pin of a specific port, different parts of the port can be configured to be controlled by either one of the two available modules or by the PIO Controller itself.

The pinout and specification for each module describes which pins a specific module uses or may use. The PIO Controller does not have to give the module control over all pins it may drive; a subset can be used. A conceptual schematic is shown in Figure 2.2 that shows an example for PORTB.

Figure 2.2: PIO Controller configuration

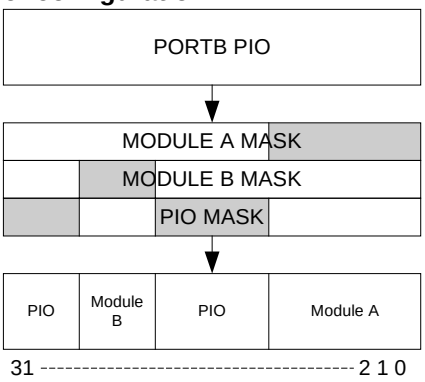


Figure 2.2 starts with a reset value for the PIO Controller and pins are controlled by the PIO Controller itself or by a module specified by the datasheet for your device. Different masks are applied for each of the two modules connected to your device as well as a PIO mask for the pins that are to be controlled by the PIO Controller. This results in the control mapping shown in the bottom.

Even though I/O pins are given exclusive rights to either the PIO Controller or one of potentially two connected modules, this can be altered "on-the-fly".

2.2 PIO Controller settings

The pins that are controlled by the PIO Controller can be used as general-purpose I/O pins. The PIO Controller has several features can be individually applied or can operate in co junction with other features to support numerous types of functionality.

2.2.1 Status, enabling and disabling functionality

The status of a specific pin or port can be read from status registers. These registers are available for all functionality applicable to the PIO Controller. This is true for the functionality described in chapter 2.4 and the trailing chapters. These registers are usually labeled as read-only.

Most of the functionality available through the PIO Controller has a disable and an enable register in addition to the status register. These registers are commonly write-only registers. The user can explicitly enable or disable features for individual pins and read the status from the corresponding status register.

2.3 Register layout

The registers described in the following chapters are all 32 bit registers. All bits reflect the pin of the port. I.e. if bit 3 of a register is set/cleared, this affects pin 3 of the actual port.

2.4 General PIO features

The functionality described in this chapter can be used independently of the module controlling the pins of a specific port.

2.4.1 I/O controller

As stated earlier, each pin can be controlled by either one of two possible modules or by the PIO Controller itself. The registers for setting up this functionality are:

Table 1: PIO setup registers

Register name	Type	Description
PER	Write-only	PIO Enable Register. Set the pin mask for PIO controlled pins here.
PDR	Write-only	PIO Disable Register. Set the pins that are not to be controlled by the PIO Controller.
PSR	Read-only	PIO Status Register.
OER	Write-only	Output Enable Register. Define the pins that are to be used as output by the PIO Controller.
ODR	Write-only	Output Disable Register. The input pins are set in this register.
OSR	Read-only	Output Status Register.
ASR	Write-only	Module A Select Register. Define the pins that are to be controlled by module A here.
BSR	Write-only	Module B Select Register. The pins that are controlled by module B are written here.
ABSR	Read-only	AB Status Register. Status for each pin; a low bit indicates that the pin is controlled by module A, while high indicated module B.

2.4.2 Pull-up enable/disable

Individual pins can either have an internal pull-up enabled or disabled. This pull-up value is typically around 10kΩ. This feature is enabled upon reset.

Table 2: Pull-up user interface

Register name	Type	Description
PUER	Write-only	Pull-Up Enable Register. Define which I/O lines that should use the internal pull-up resistor
PUDR	Write-only	Pull-Up Disable Register. Disable internal pull-up on these lines
PUSR	Read-only	Pull-Up Status Register. Shows which lines has internal pull-up switched on (high) and which doesn't (low).

2.5 PIO output

This chapter describes typical functionality for PIO lines used as output lines.

2.5.1 Data control

Bits part of a port can explicitly be set or cleared via the Set Data Output Register (SODR) or Clear Data Output Register (CODR). The status can be read from the Output Data Status Register (ODSR).

Table 3: Data control registers

Register Name	Type	Description
SODR	Write-only	Set Output Data Register. The bitfield written to this register sets the corresponding pins for the port.
CODR	Write-only	Clear Output Data Register. Clears the corresponding bits for the port.
ODSR	Write-only or Read/Write	Output Data Status Register. This is by default Read-only and shows the pin status.
OWER	Write-only	Output Write Enable Register. Enables write access to the ODSR register
OWDR	Write-only	Output Write Disable Register. Disables write access to the ODSR register
OWSR	Read-only	Output Write Status Register. Indicates which pins are writeable from ODSR register.

Note that the registers OWER and OWDR can enable direct write operations through the ODSR register.

2.6 PIO input

Some features are typically used when PIO lines are used as input lines. This chapter covers these features.

2.6.1 Input Change Interrupts

Individual pins can be used as an interrupt source. This is a level change interrupt. An appropriate interrupt handler must be applied to utilize this feature. Note: This functionality can be used even though the pin is configured as a PIO output pin, or under control of an I/O module.

Table 4: Interrupt control registers

Register Name	Type	Description
IER	Write-only	Interrupt Enable Register. Enable interrupt Change on the I/O line.
IDR	Write-only	Interrupt Disable Register. Disable Interrupt Change on the I/O line.
IMR	Read-only	Interrupt Mask Register. Show which I/O lines that have interrupt change enabled (high) and which are disabled (low).
ISR	Read-only	Interrupt Status Register. Shows if one or more interrupts have been trigged on the I/O lines since the last read of this register.

2.6.2 Glitch input filters

Quick transitions may occur on an input line. These transitions may be neglected by applying a glitch input filter on appropriate pins. For a level change to be visible by the PIO controller, the level change must be equal or longer than 1 master clock cycle. Pulses smaller than ½ master clock cycle are automatically neglected. Pulses between ½ and 1 master clock cycles may be neglected depending on the precise timing of the occurrence.

Table 5: Glitch filter user interface

Register name	Type	Description
IFER	Write-only	Input Filter Enable Register. Enables the glitch filter on the corresponding I/O pins
IFDR	Write-only	Input Filter Disable Register. Disables the glitch filter for the corresponding I/O pins
IFSR	Read-only	Input Filter Status Register. Shows which I/O pins that have the glitch filter turned on.

3 Example code

Examples are available from the corresponding driver package. Several examples are available, describing and showing various PIO Controller features.

3.1 Documentation

Function specific documentation is available in the package. Refer to readme.html in the source code directory.

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